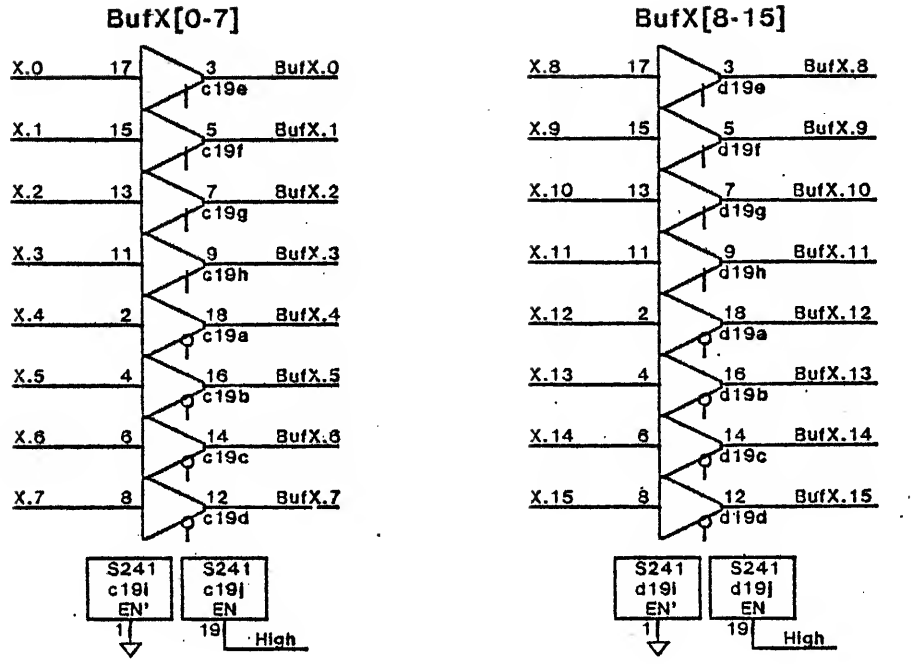
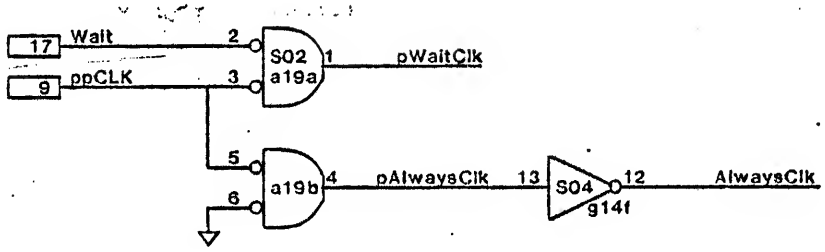
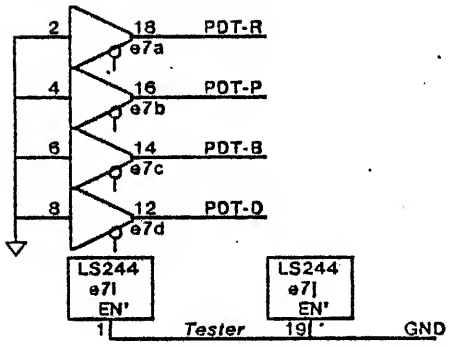
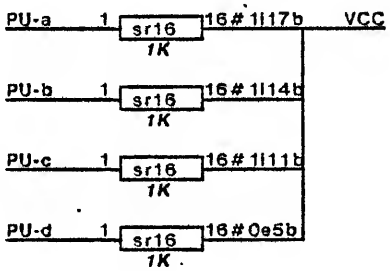
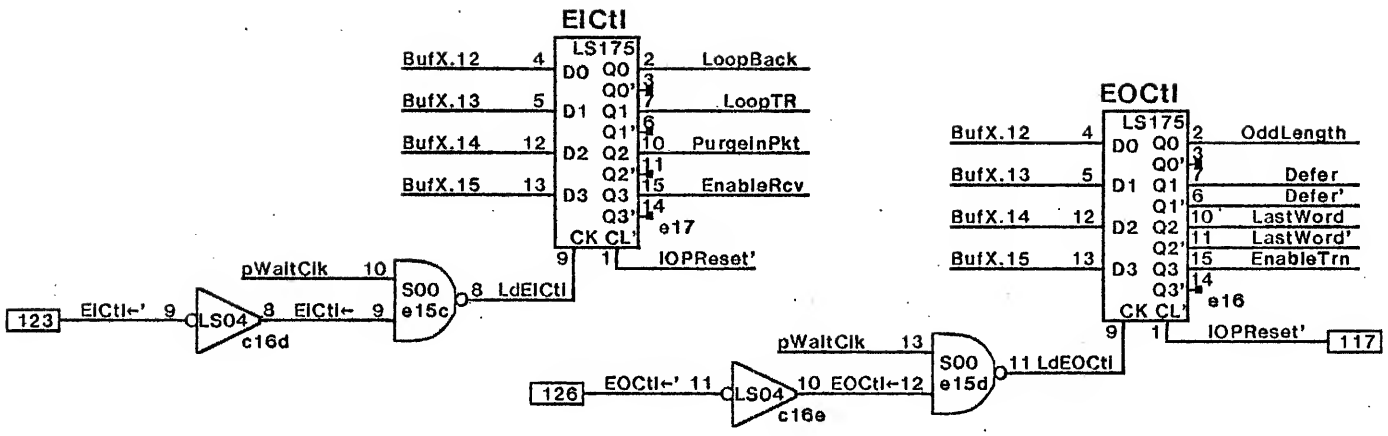


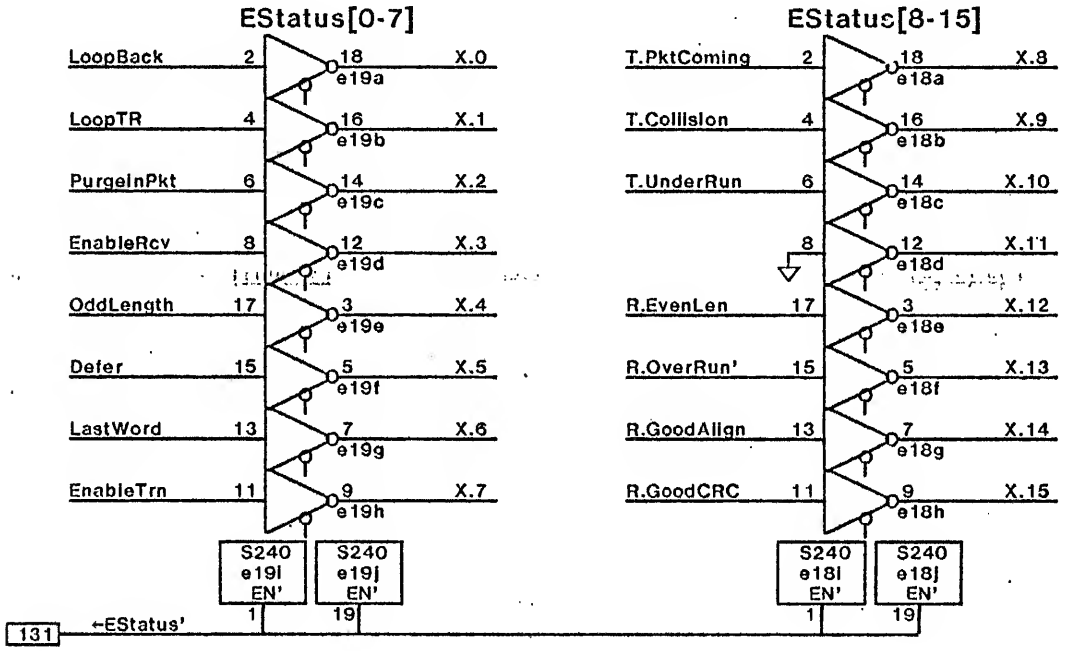


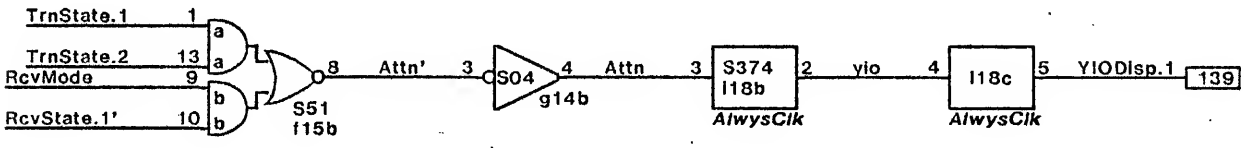


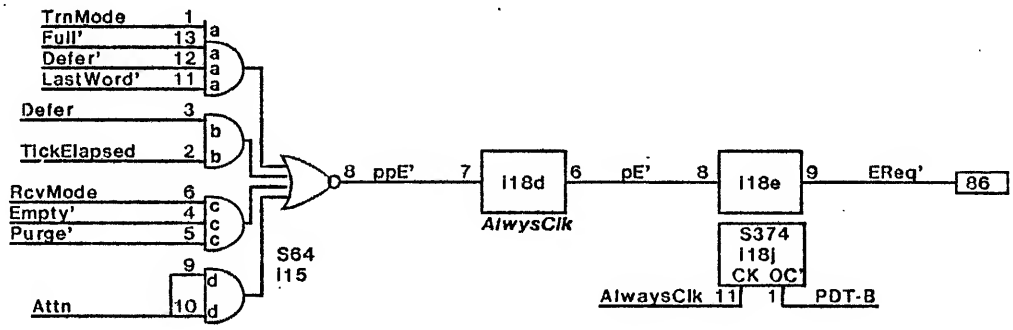


XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dandelion	CP Clocks & Buffered X-bus Testabilty, Pullups	Option01.sil	Garner	C	7/30/80	01

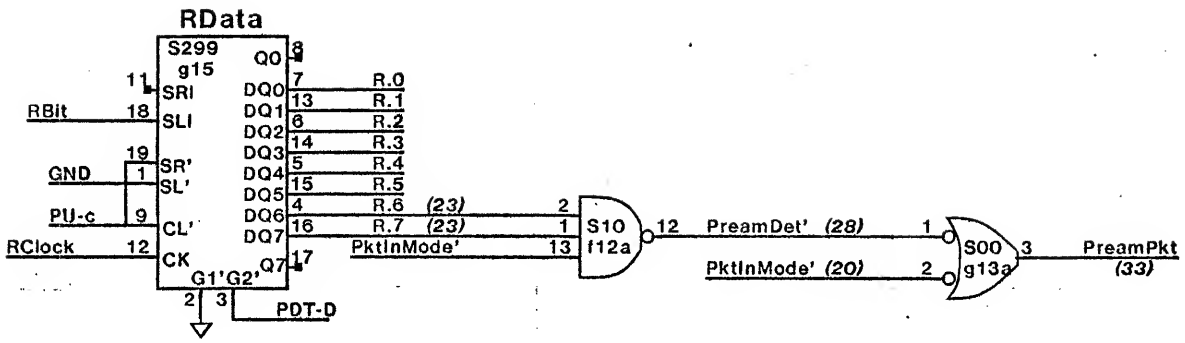


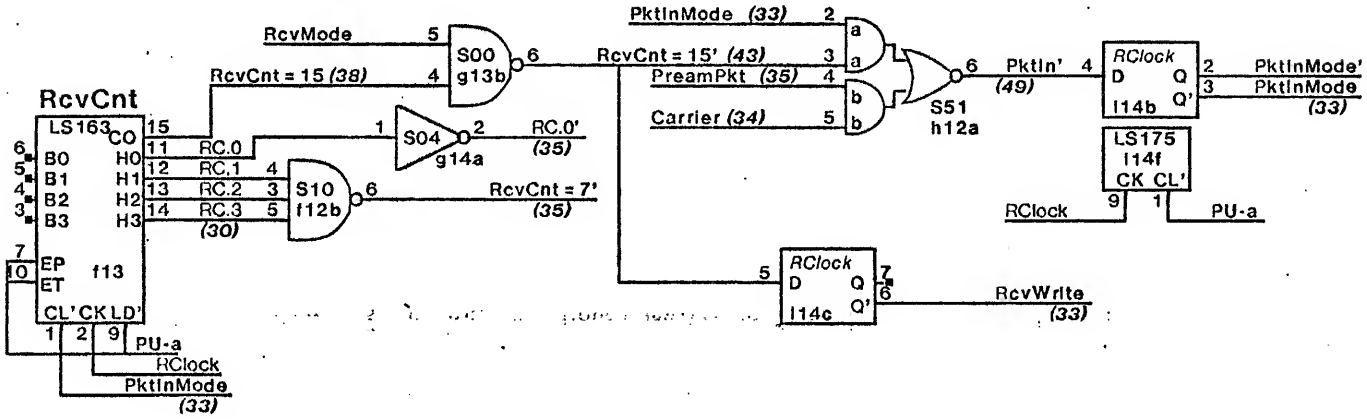


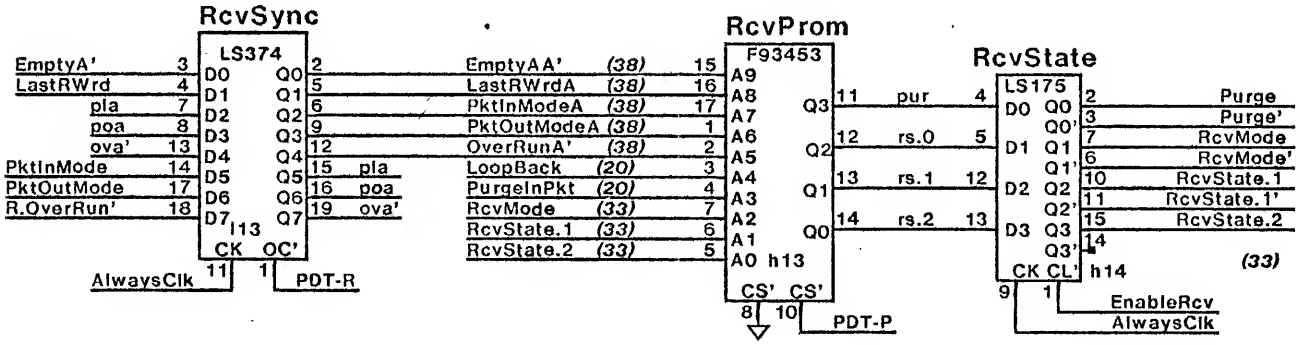




XEROX SDD	Project: Dandelion	CP Interface	File: Option02.sil	Designer: Garner	Rev: C	Date: 7/30/80	Page: 02





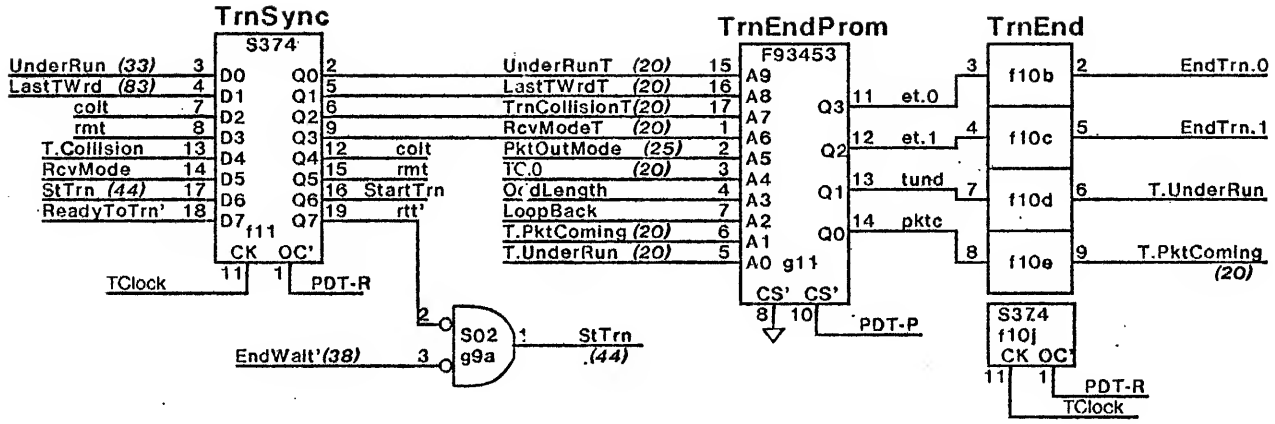


States **Outputs**

0	*Off*		
1	*unused*		RdLastWrd
2	*Skip (wait for no Carrier)*		
3	*Idle (wait for PktInMode)*		
4	*Post Status*	RcvMode InAttn	
5	*ReadLastWord*	RcvMode InAttn	RdLastWrd
6	*Purge*	RcvMode Purge	
7	*PktInMode*	RcvMode	

Loopback: skip & idle until PktOutMode true
~Loopback: remain off if PktOutMode true
Remain in PktInMode if (PktInMode OR ~Empty)

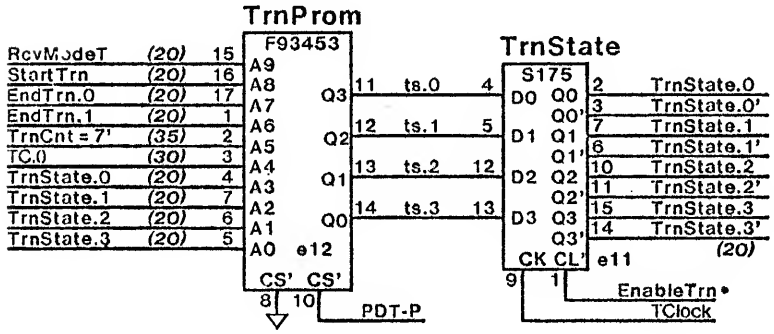
XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dandelion	Receive Data/States	Option03.sil	Garner	C	7/30/80	03

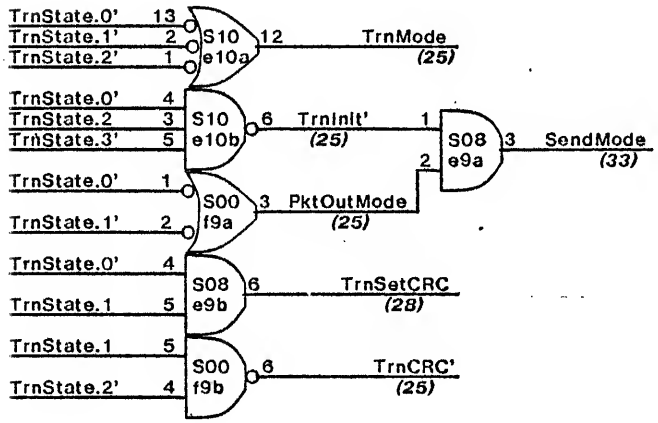


EndTrn

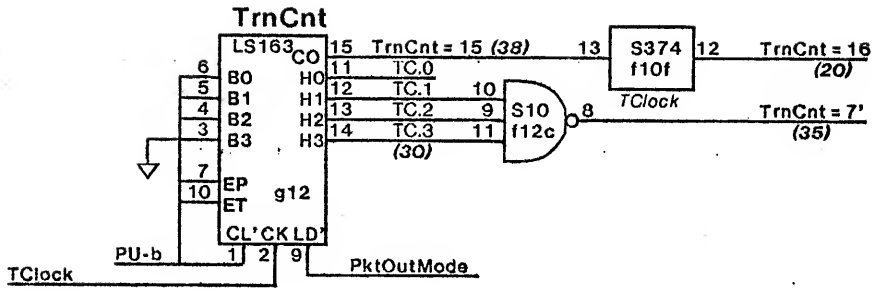
- *0 EndWithCRC = ~Loopback AND LastByte*
- *1 EndWithoutCRC = (Loopback AND LastByte) OR RcvMode*
- *2 EndWithJam = T.UnderRun OR TrnCollision*
- *3 unused*

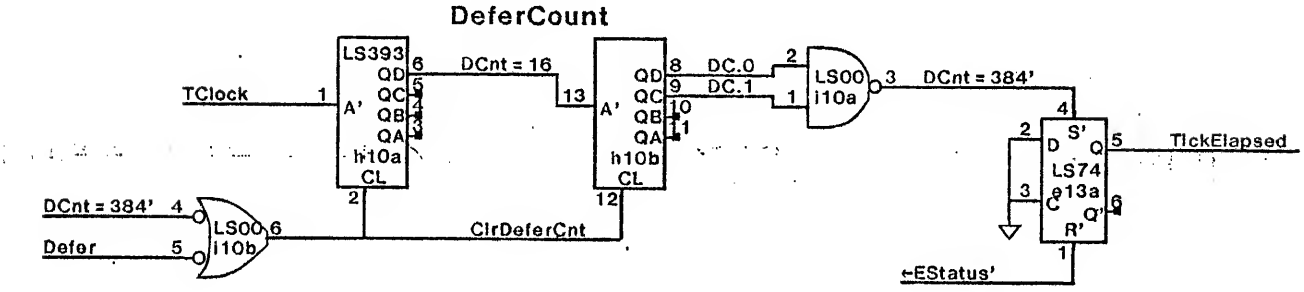
LastByte = LastTWrd AND (TC.0 XOR OddLength)
T.UnderRun = T.UnderRun OR UnderRun
T.PktComing = T.PktComing OR RcvMode

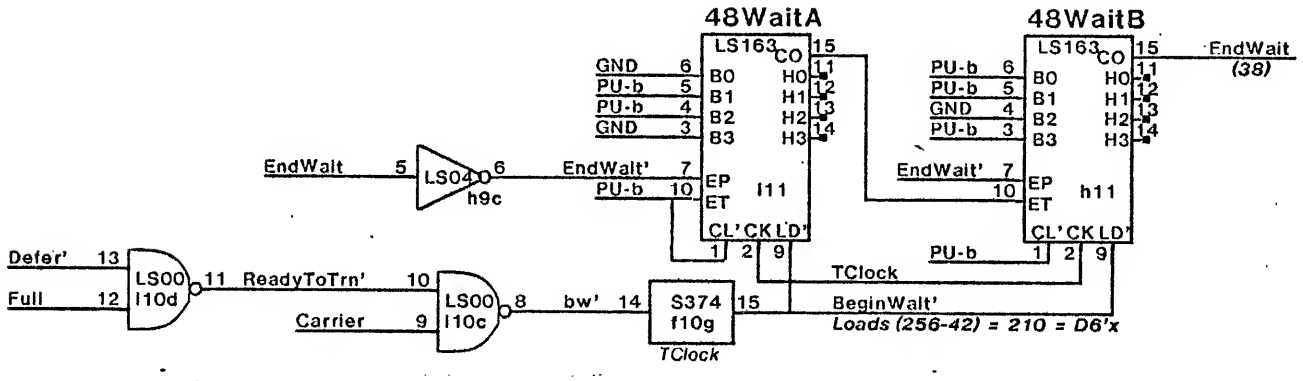




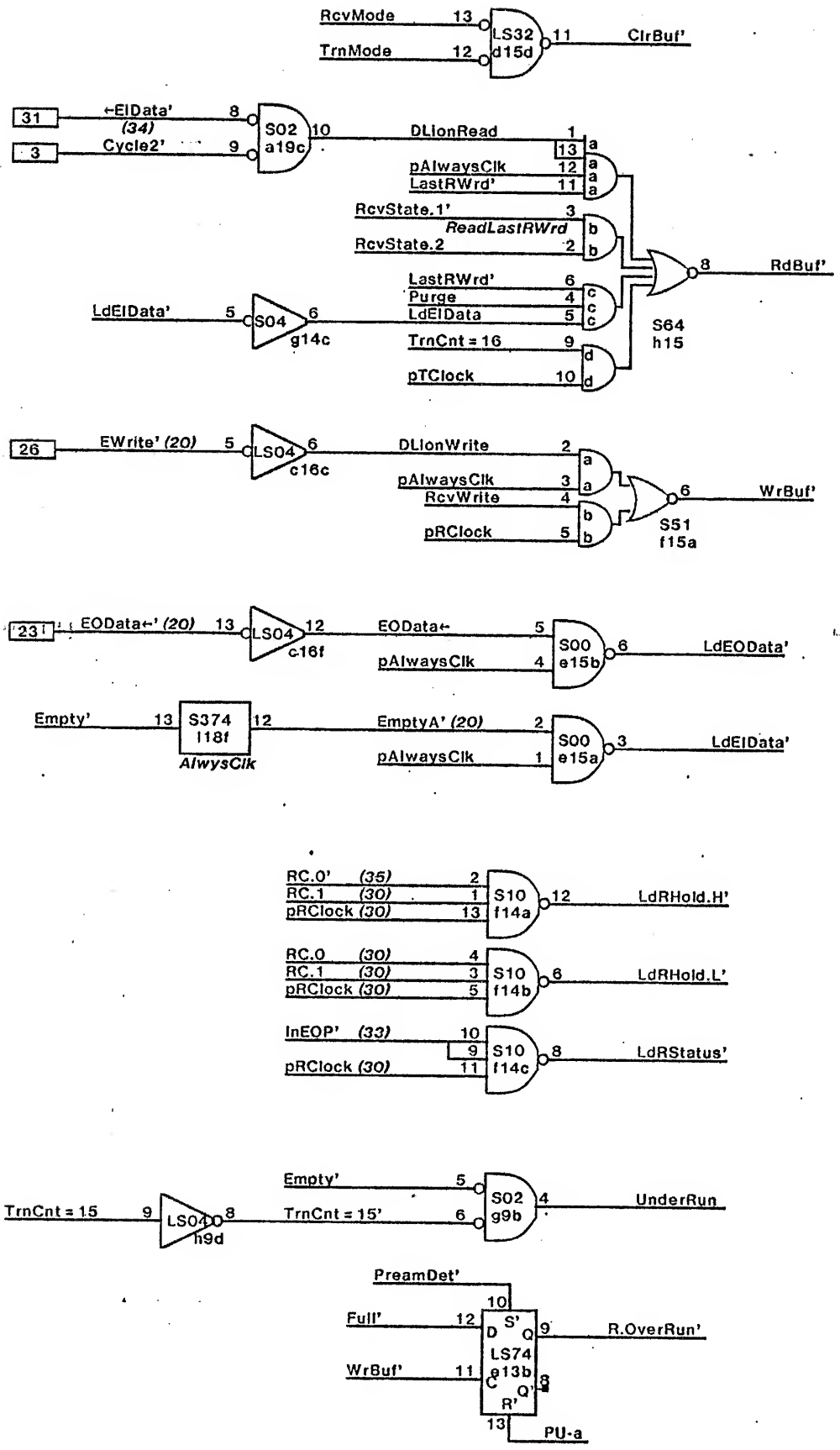
States		*Outputs*				
0	*Off*					
1	*WaitForService*					
2	*WaitToTran*	TrnMode				TrnInit
3	*PostOutStatus*	TrnMode				OutAttn
4	*Preamb (word)*	TrnMode	PktOutMode	Send	SetCRC	
5	*Preamb 1 (word)*	TrnMode	PktOutMode	Send	SetCRC	
6	*TrnInitialize*	TrnMode	PktOutMode		SetCRC	TrnInit
7	*Jam2 (word)*	TrnMode	PktOutMode	Send	SetCRC	OutAttn
8	*CRC0 (byte)*	TrnMode	PktOutMode	Send	TrnCRC	
9	*CRC1 (byte)*	TrnMode	PktOutMode	Send	TrnCRC	
10	*Send*	TrnMode	PktOutMode	Send		
11	*Jam1 (word)*	TrnMode	PktOutMode	Send		OutAttn
12	*CRC3 (byte)*	TrnMode	PktOutMode	Send	TrnCRC	
13	*CRC2 (byte)*	TrnMode	PktOutMode	Send	TrnCRC	
14	*Jam0 (word)*	TrnMode	PktOutMode	Send		
15	*Jam3 (1 bit)*	TrnMode	PktOutMode	Send		OutAttn



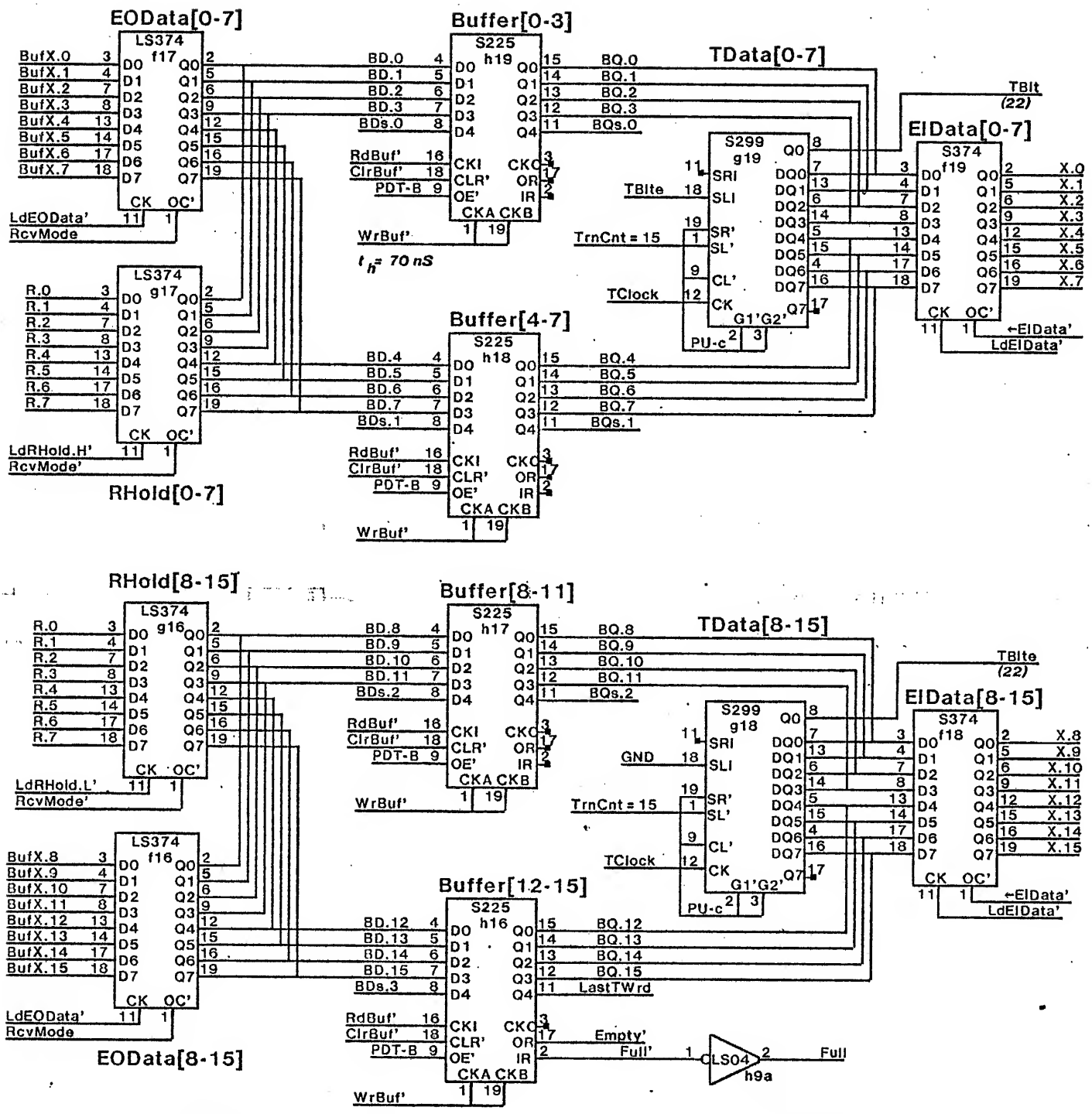




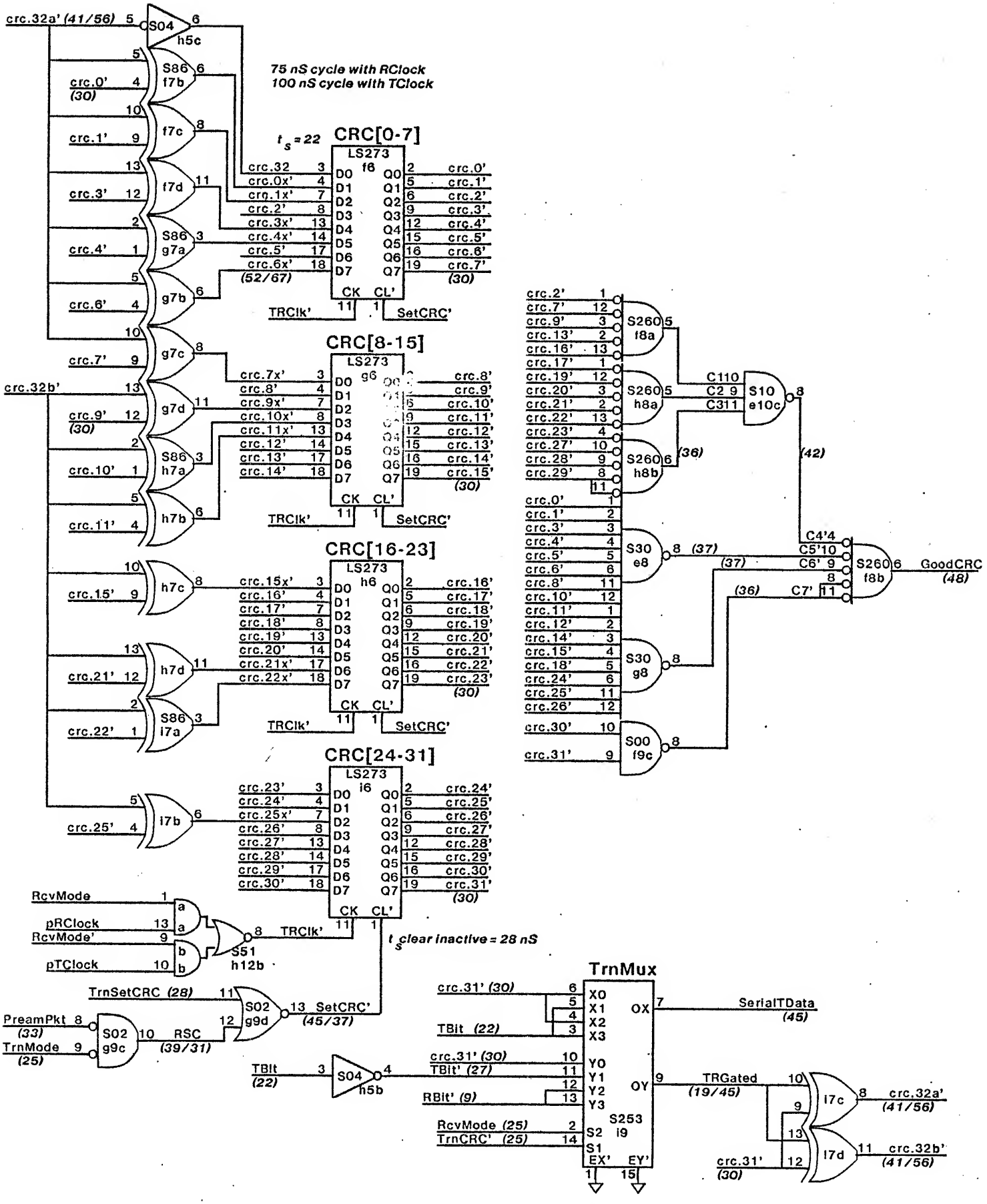
XEROX SDD	Project Dandelion	Transmit Counters	File Option05.sil	Designer Garner	Rev C	Date 7/30/80	Page 05



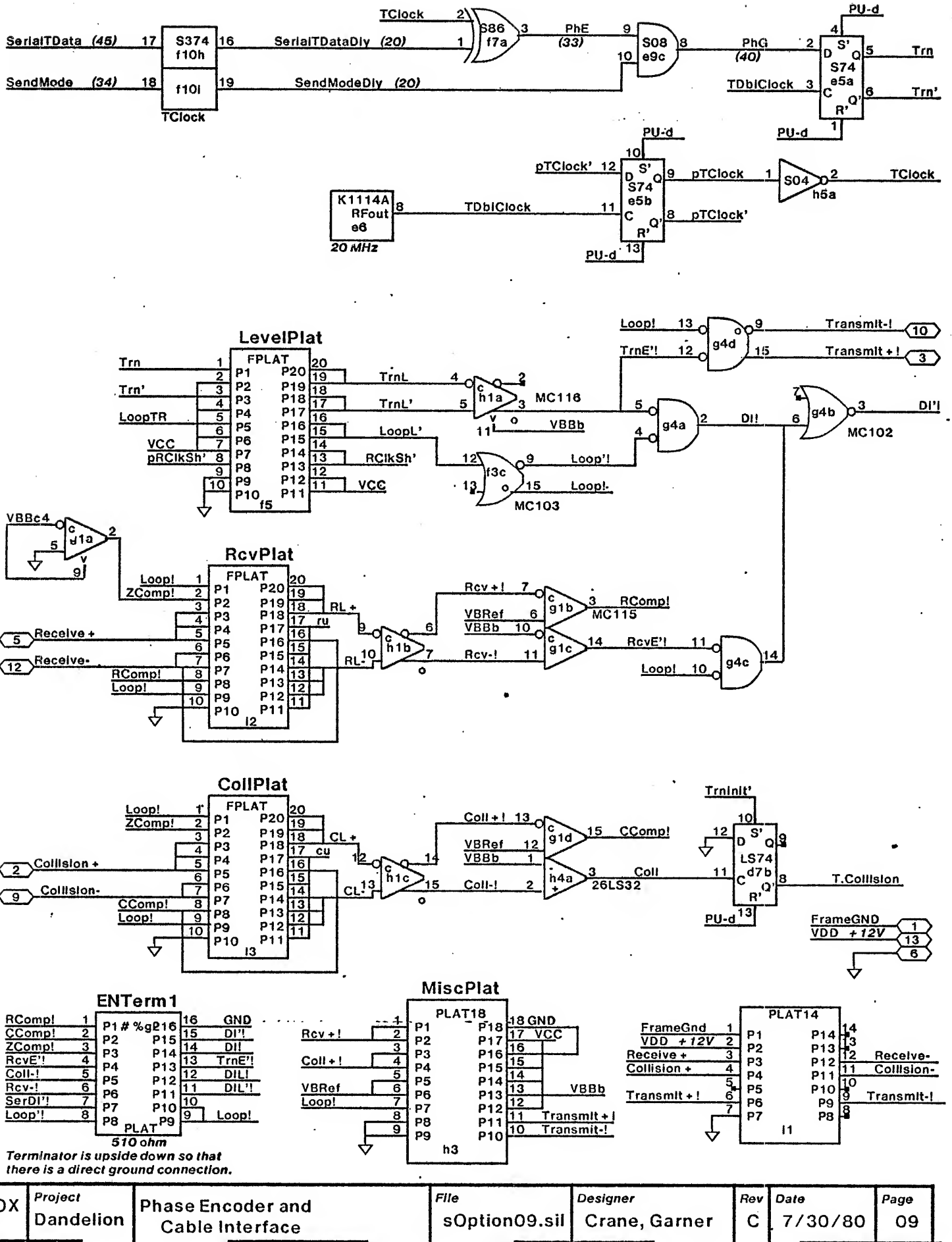
XEROX SDD	Project Dandelion	Buffer Control & Status	File Option06.sil	Designer Garner	Rev C	Date 7/30/80	Page 06



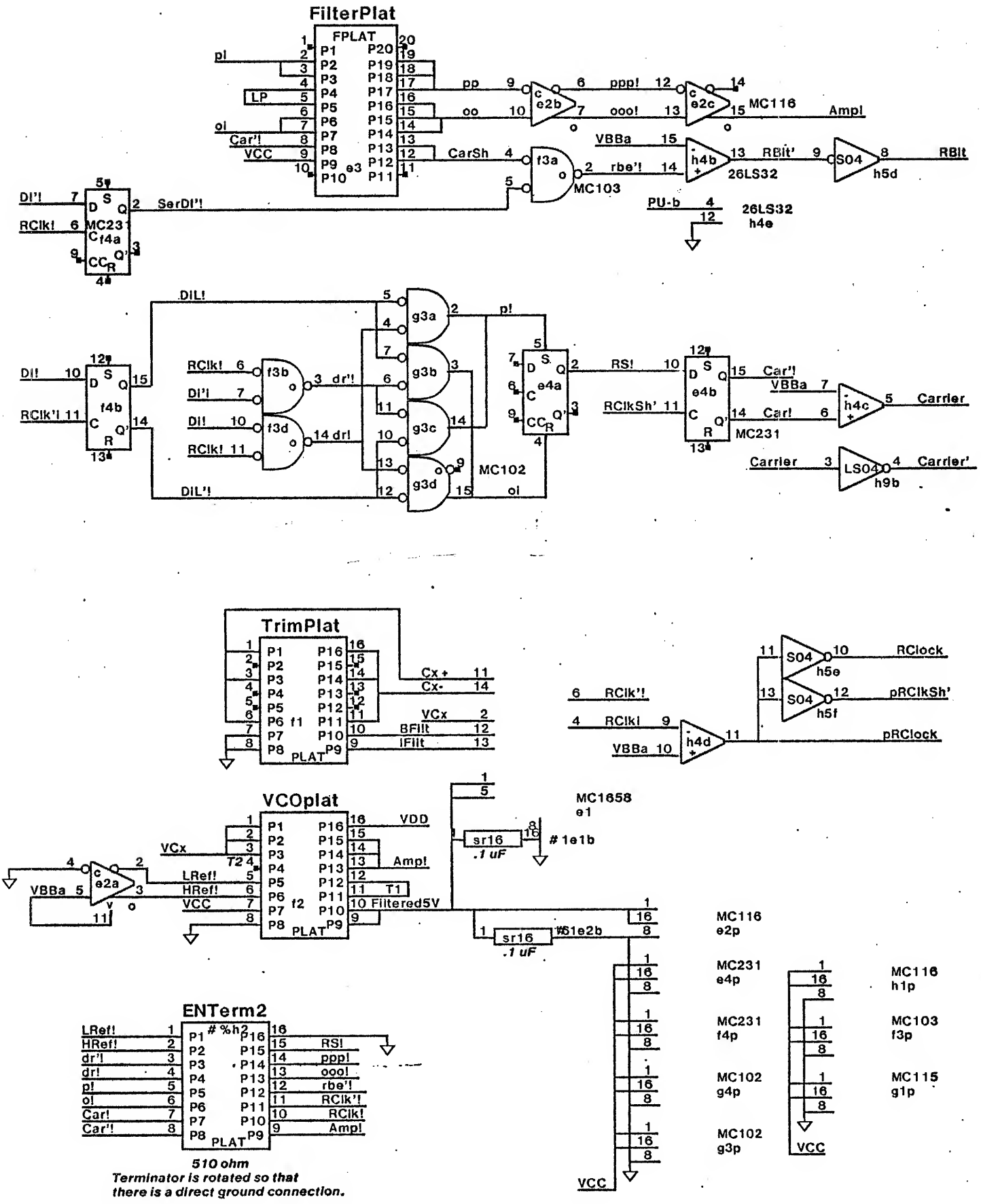
XEROX SDD	Project: Dandelion	Half Duplex Buffer	File: Option07.sil	Designer: Garner	Rev: C	Date: 7/30/80	Page: 07



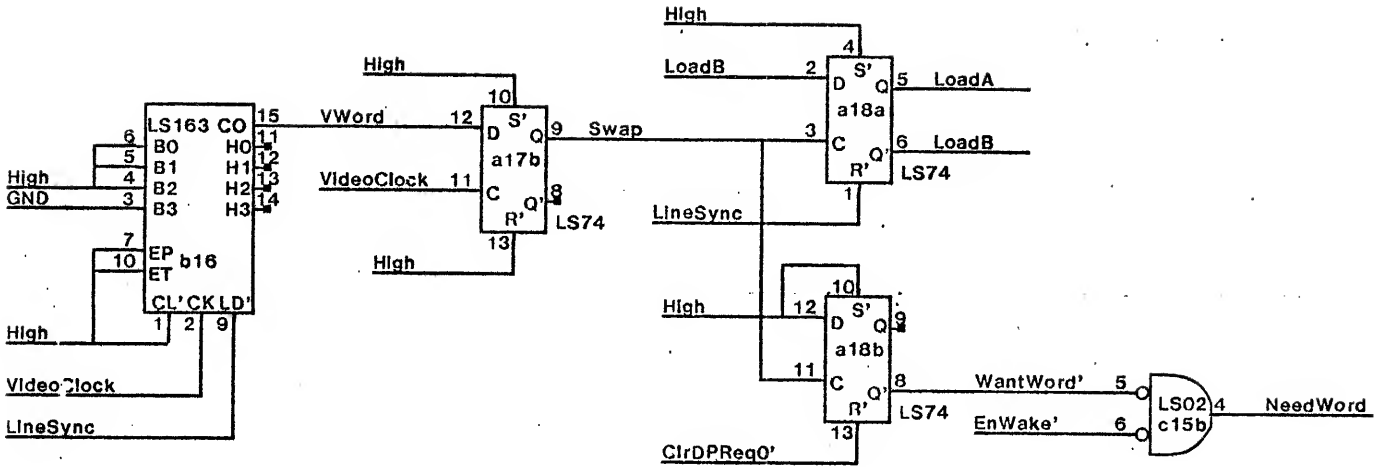
XEROX SDD	Project: Dandelion	CRC	File: Option08.sil	Designer: Garner	Rev: C	Date: 7/30/80	Page: 08

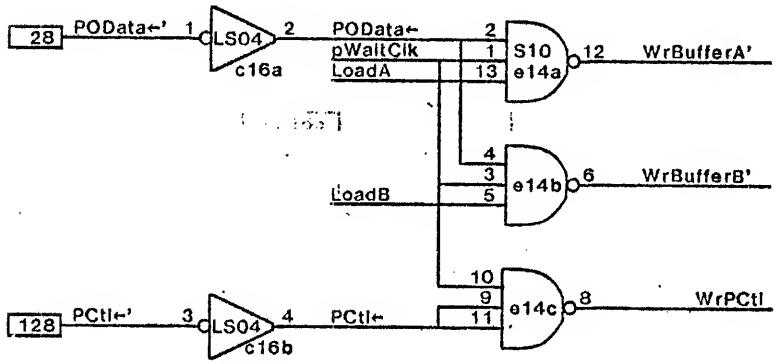


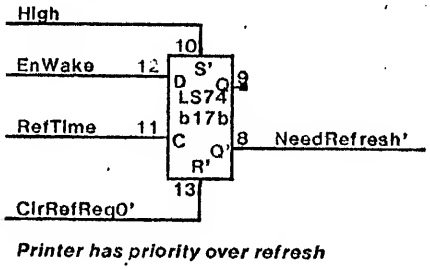
XEROX SDD	Project: Dandelion	Phase Encoder and Cable Interface	File: sOption09.sil	Designer: Crane, Garner	Rev: C	Date: 7/30/80	Page: 09



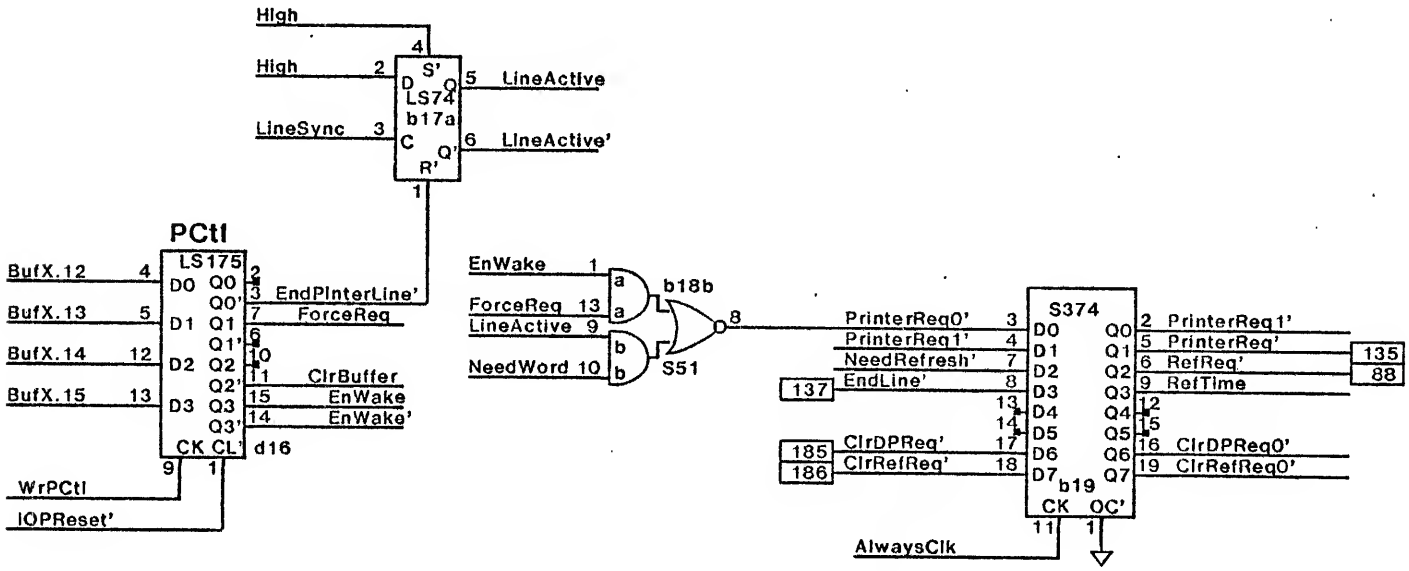
XEROX SDD	Project: Dandelion	PLL Receiver	File: sOption10.sil	Designer: Crane, Garner	Rev: C	Date: 7/30/80	Page: 10



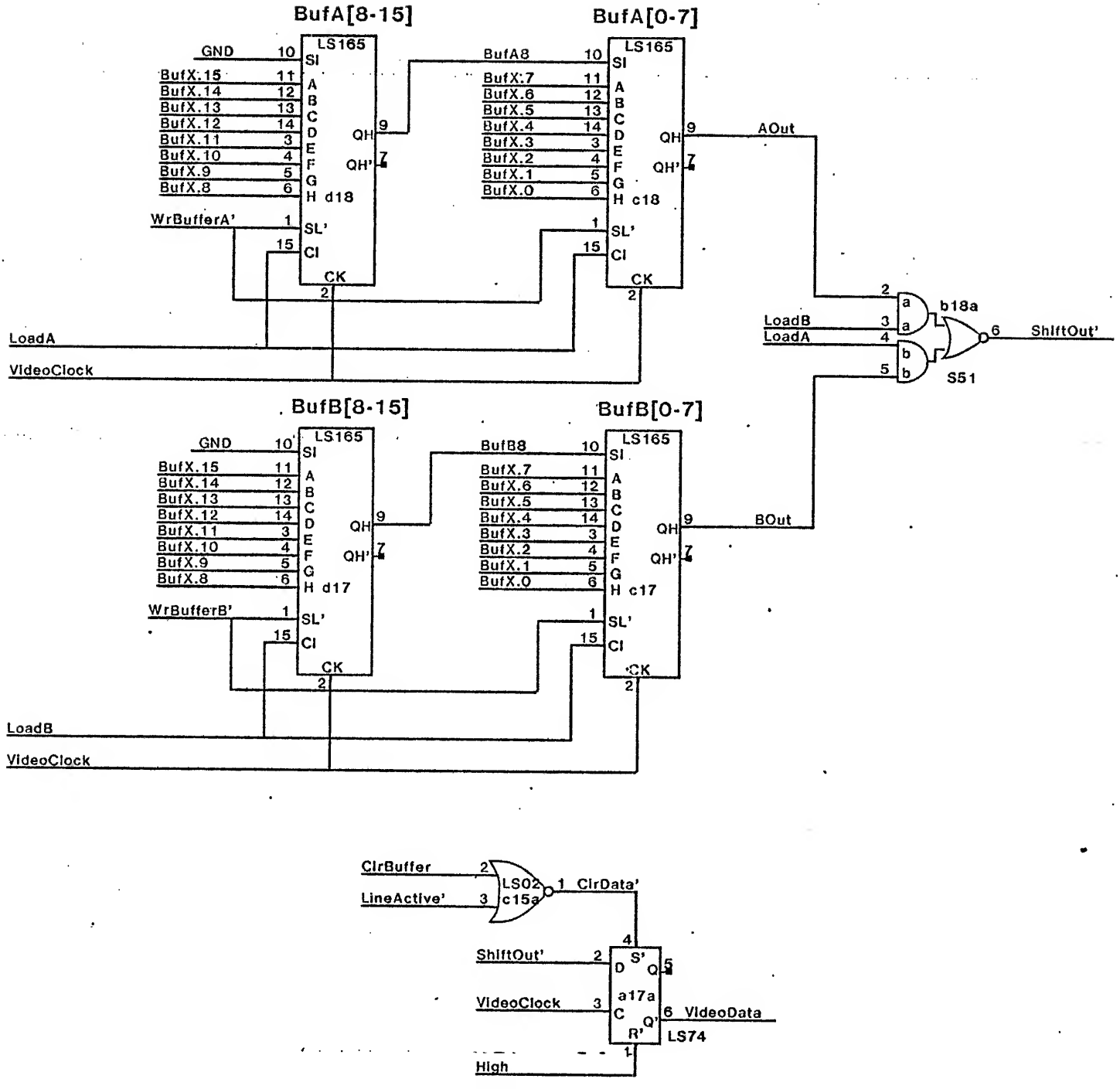




Printer has priority over refresh

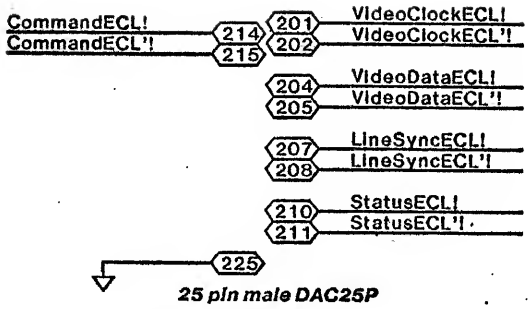


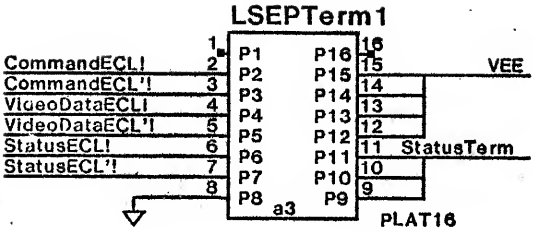
XEROX SDD	Project: Dandelion	LSEP Wakeup Logic	File: Option20.sil	Designer: Jarvis	Rev: C	Date: 7/30/80	Page: 20

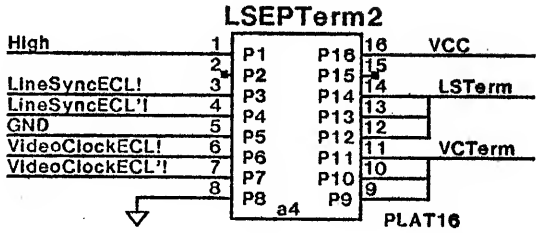


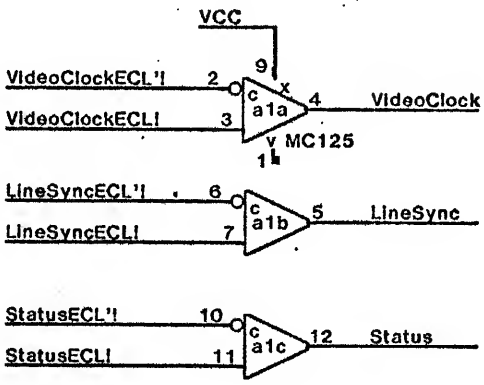
Reclocking the data avoids glitches at word boundaries

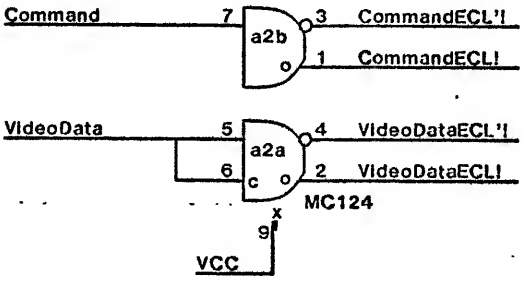
XEROX SDD	Project		File	Designer	Rev	Date	Page
	LSEP	LSEP Shifters	Option21.sil	Jarvis	C	7/30/80	21



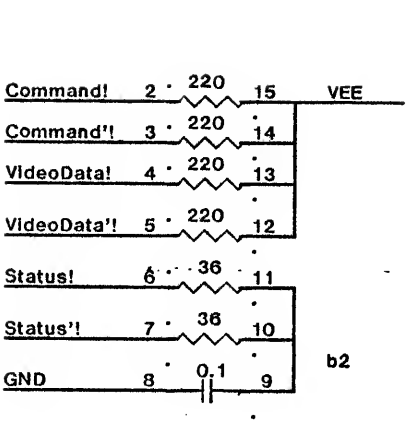


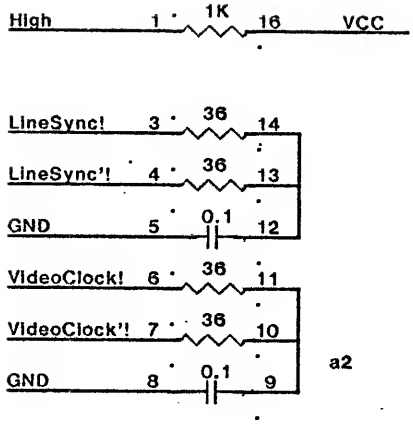






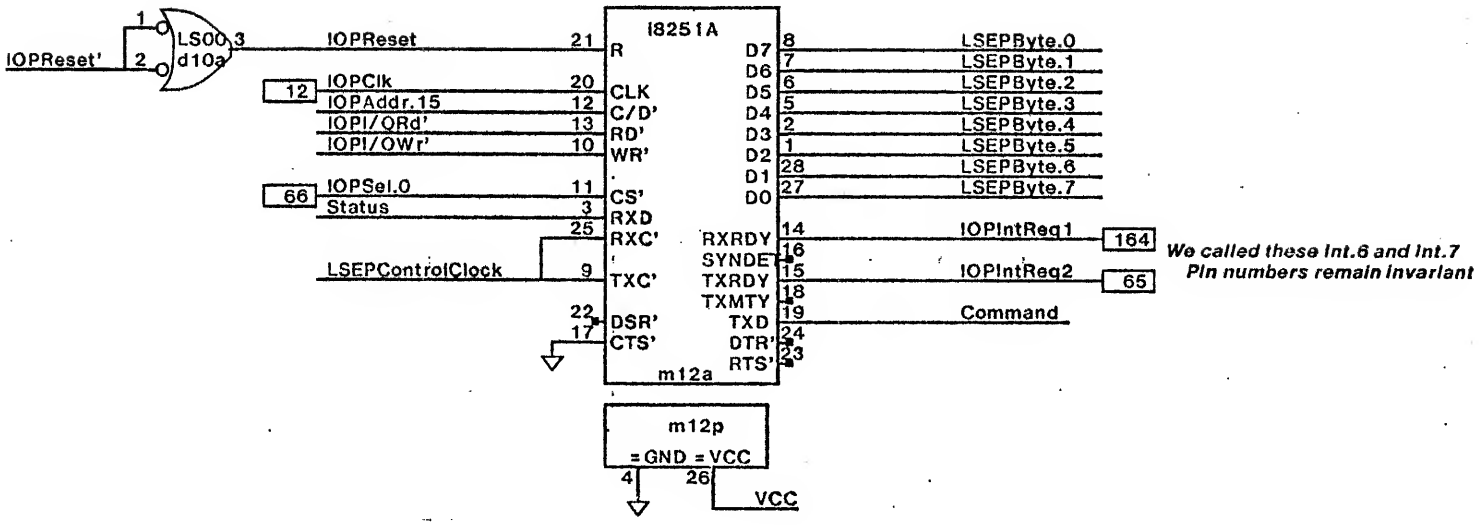
XEROX SDD	Project Dandelion	LSEP Printer Connector	File sOption22.sil	Designer Jarvis	Rev C	Date 7/30/80	Page 22

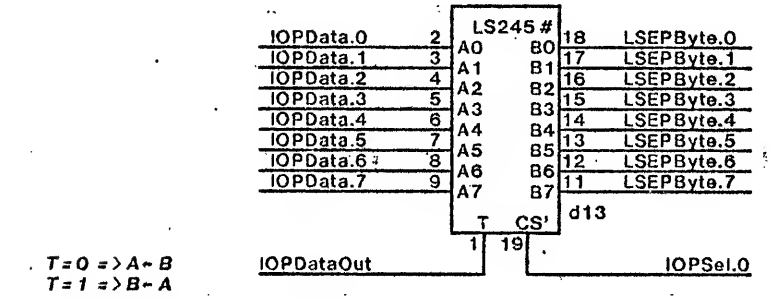




XEROX SDD	Project	Reference	File	Designer	Rev	Date	Page
	Dandelion	LSEP Terminators	pOption22.sil	Jarvis	C	7/8/80	22

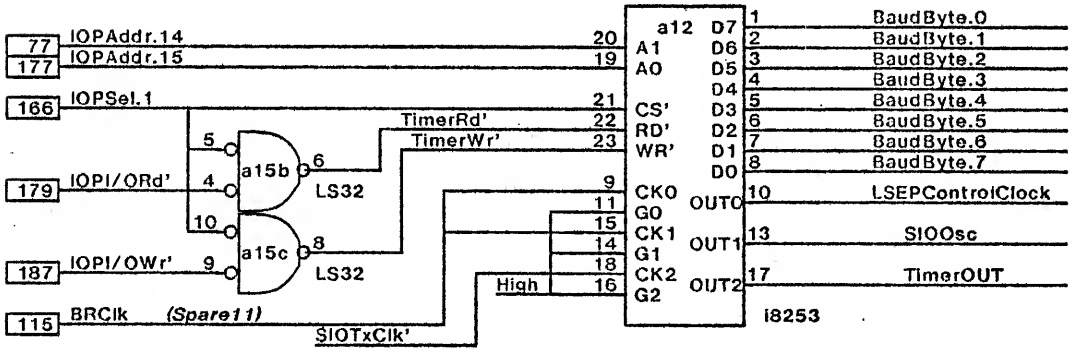
LSEP UART

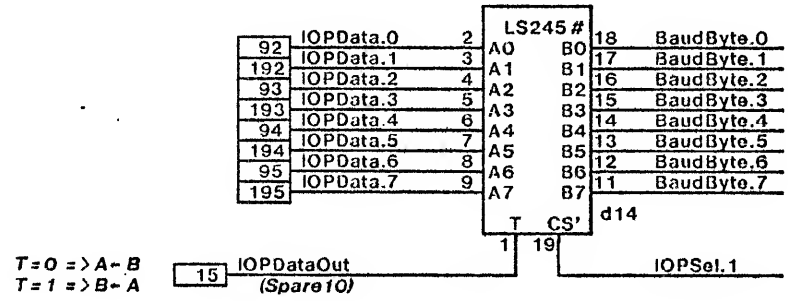




Note: Due to a design shortcoming the RD' and WR' lines of the 8253-5 must be externally qualified.

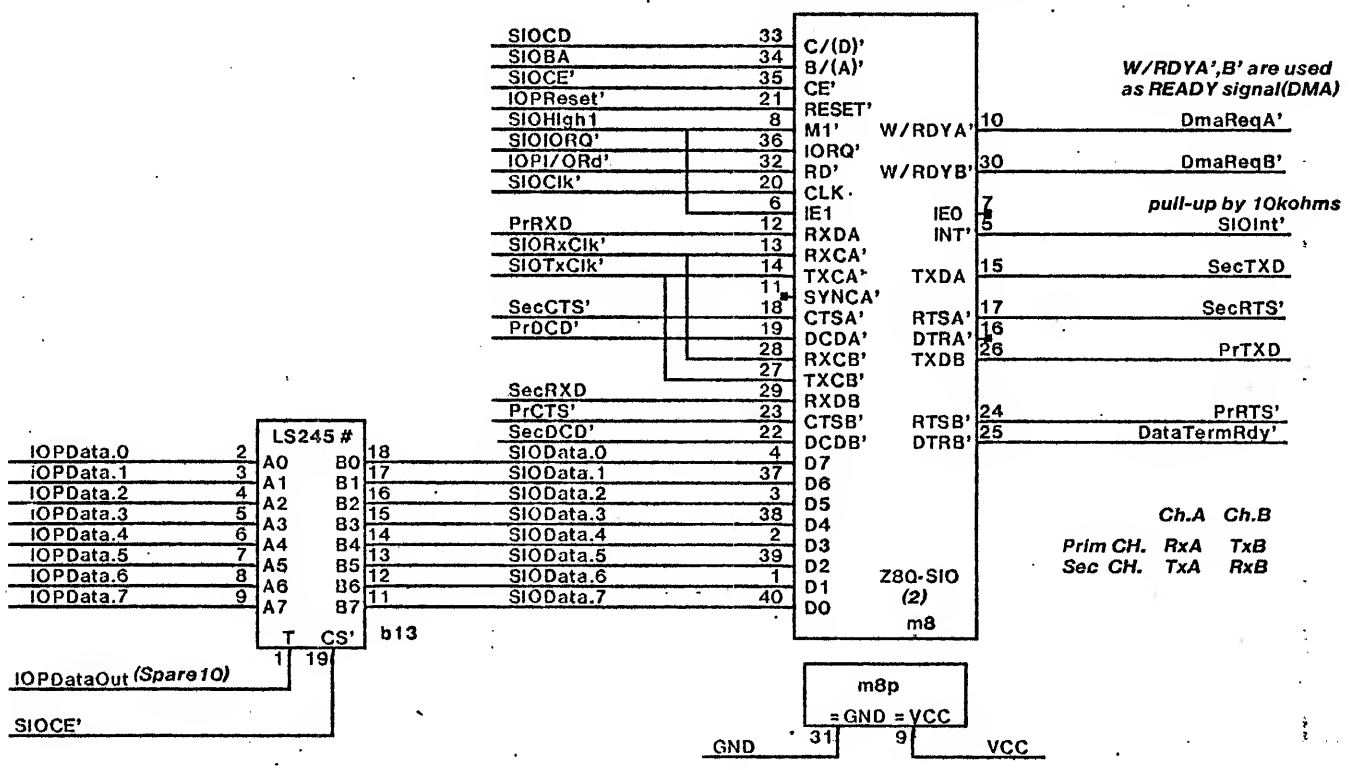
Baud-rate generator



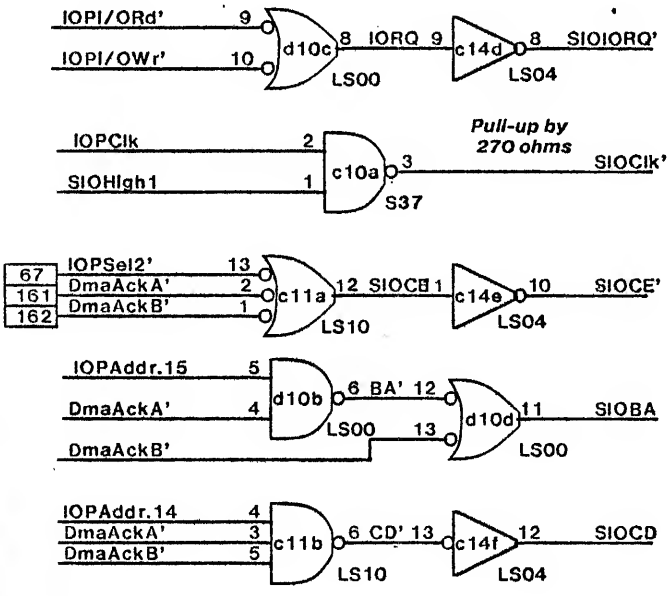


XEROX SDD	Project: Dandelion	LSEP Control and Status	File: Option23.sil	Designer: Jarvis	Rev: C	Date: 7/30/80	Page: 23

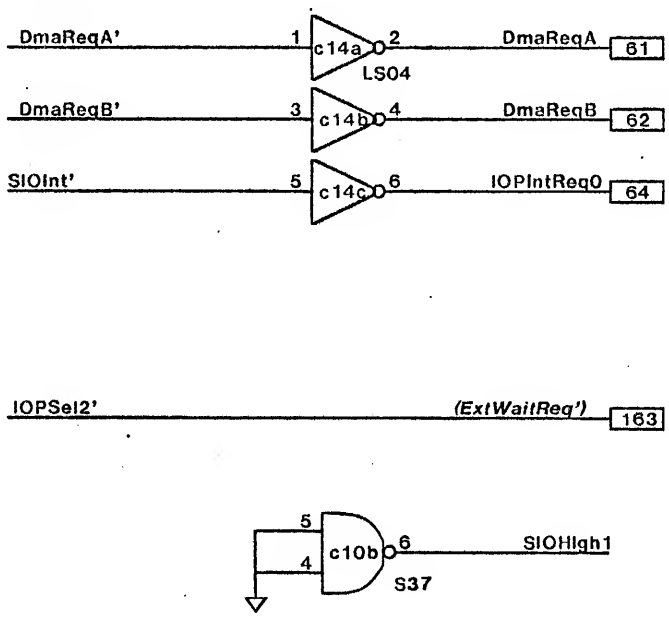
Serial I/O Controller



From 8085 *To Z80-SIO*

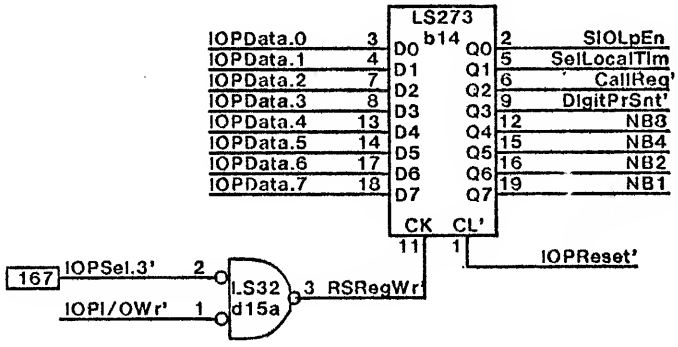


From Z80-SIO *To 8085*

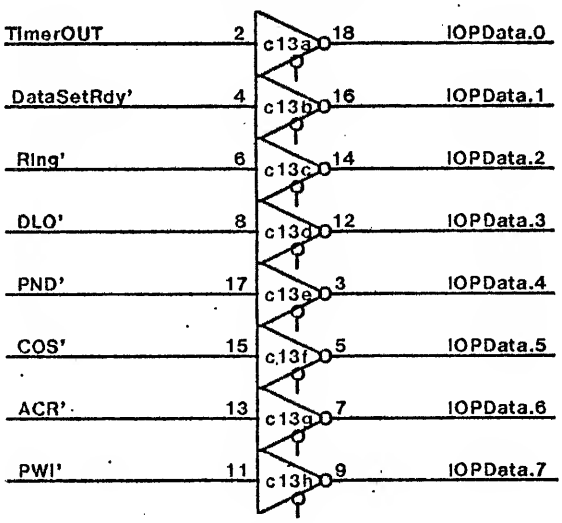


XEROX SDD	Project: Dandelion	RS-232-C Interface Z80-SIO/2, 8085 Converter	File: Option30.sil	Designer: K.Yamanaka	Rev: C	Date: 7/30/80	Page: 30

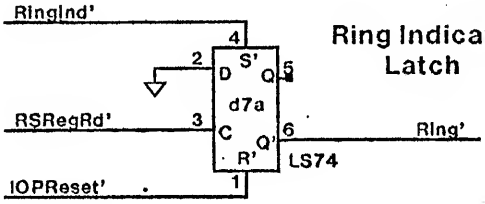
RS366 Control Register



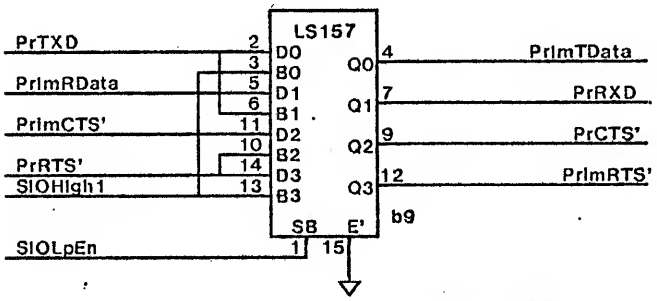
RS366 Status

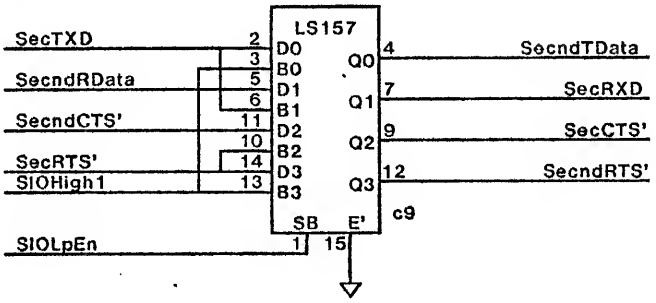


Ring Indicator Latch

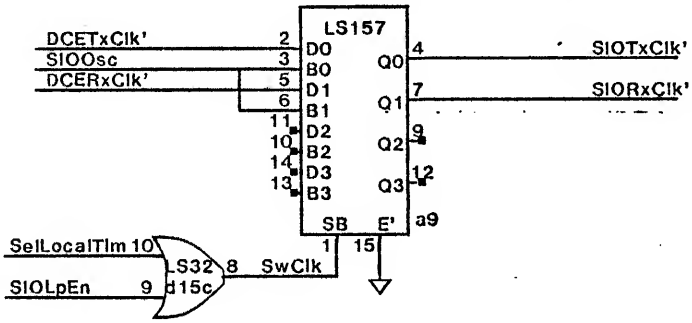


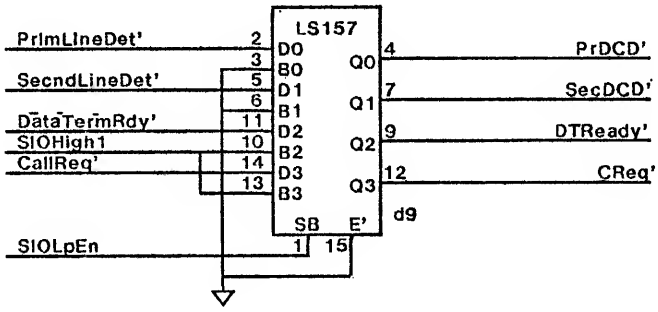
Diag Loop-Back MPX





Clock Switch

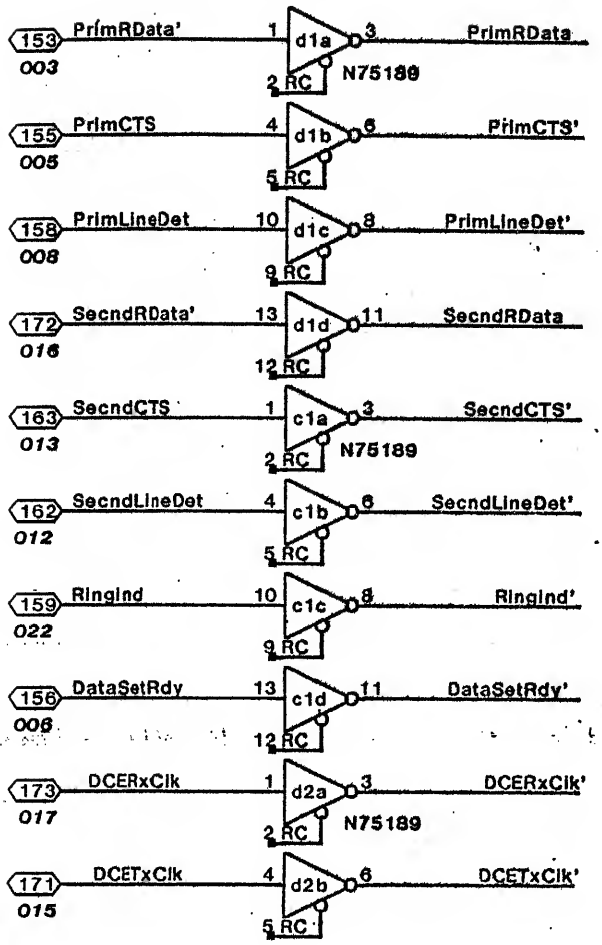




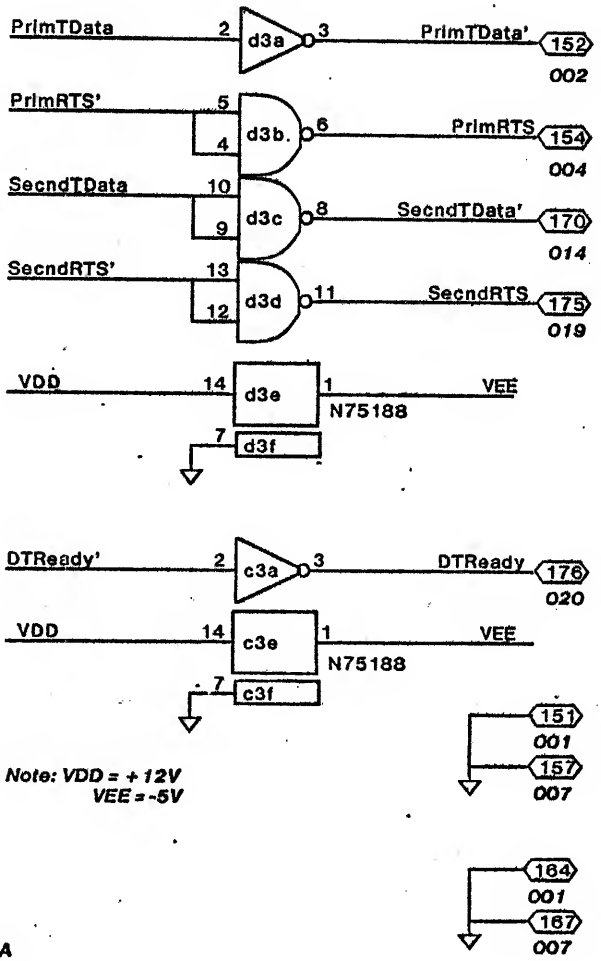
XEROX SDD	Project: Dandelion	RS366 Control & Status Diag Loop-Back MPX	File: Option31.sil	Designer: K.Yamanaka	Rev: C	Date: 7/30/80	Page: 31

RS232C Receivers

Font 2 is RS232C EIA interface pin # (DTE).

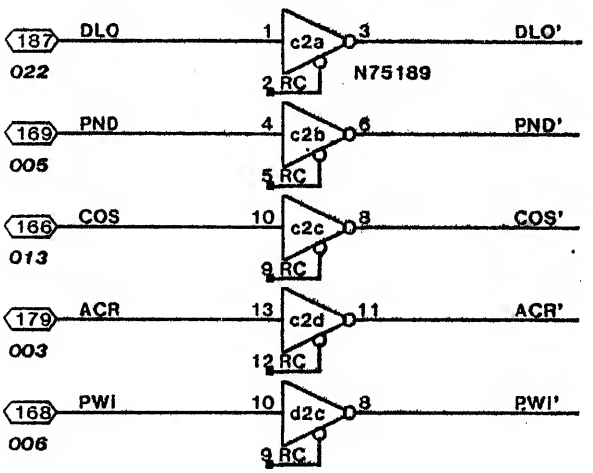


RS232C Drivers

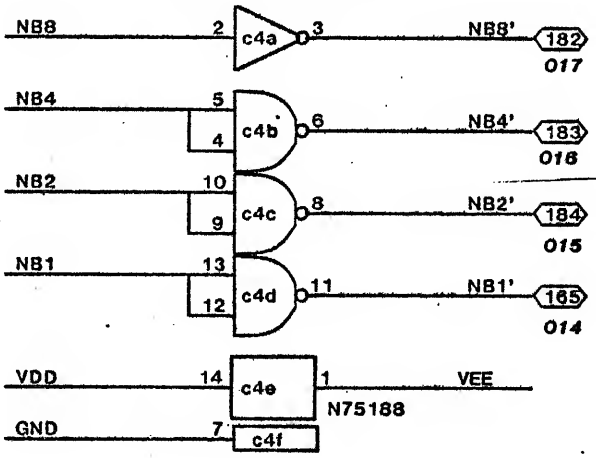


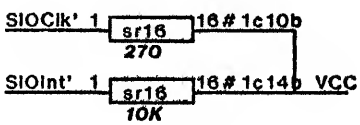
Font 2 is RS366 EIA interface pin #(DTE).

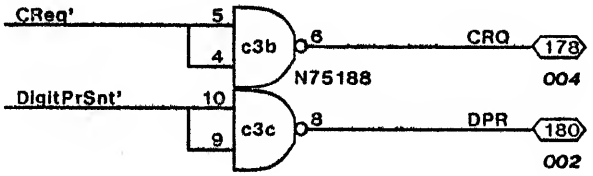
RS366 receivers



RS366 Drivers

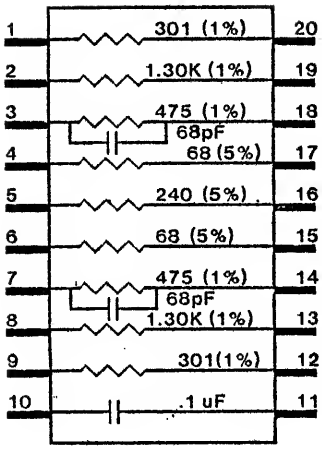




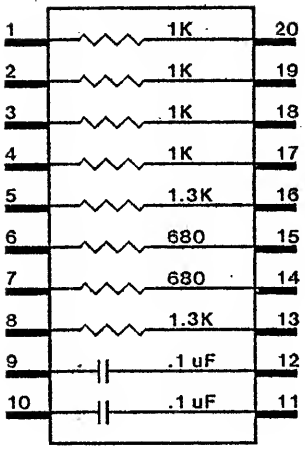


XEROX SDD	Project Dandelion	RS-232-C Driver/Receiver RS366 Driver/Receiver	File sOption32.sil	Designer K.Yamanaka	Rev C	Date 7/30/80	Page 32

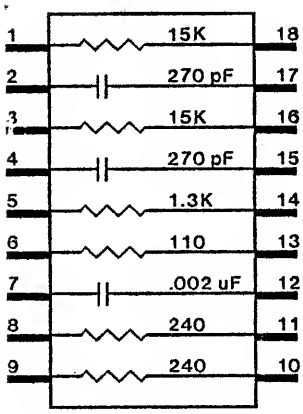
CollPlat
RcvPlat



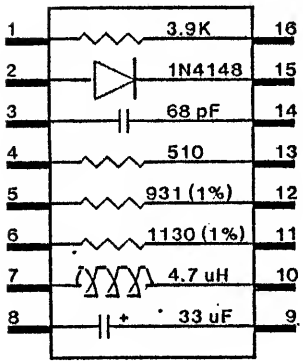
LevelPlat



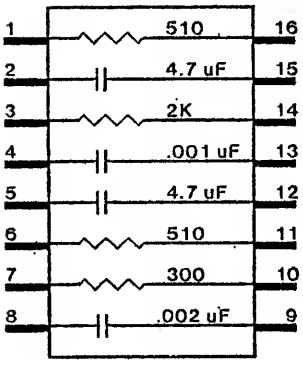
MiscPlat



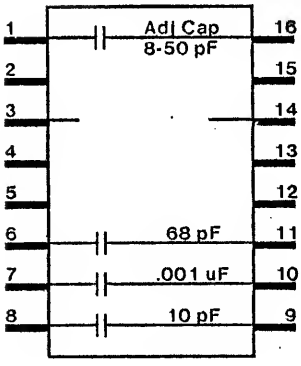
VCOPlat



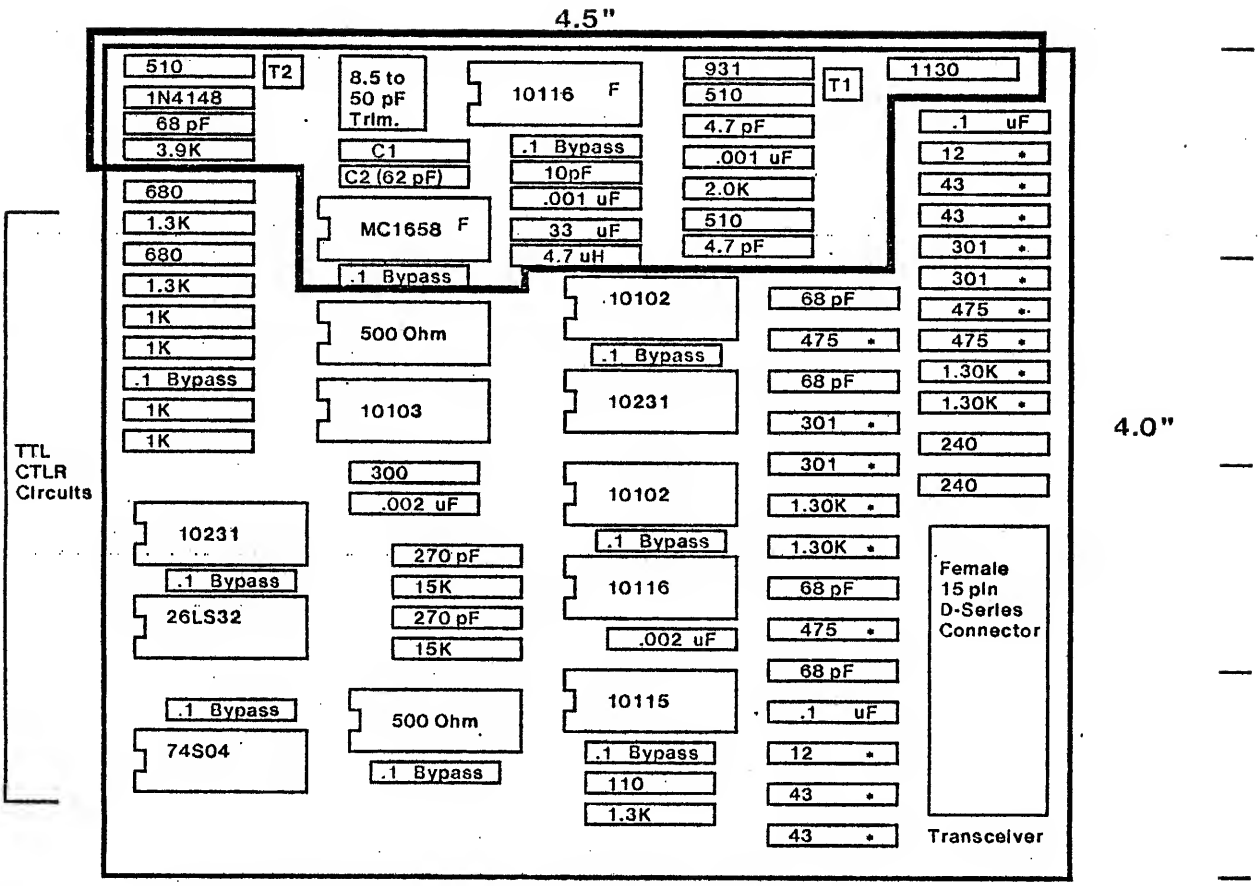
FilterPlat



TrimPlat



XEROX SDD	Project: Dandelion	Ethernet PLATs	File: Option50.sily	Designer: Garner	Rev: A	Date: 6/22/80	Page: 50



* These components will be put into a 16 pin resistor package.
F The amplifier (10116) and VCO (MC1658) chips get filtered +5 volt power.

PC Board Considerations:

1. TTL signals should only touch the periphery of this circuit. TTL-ECL conversion (resistor dividers) should be at edge of circuit as well as ECL-TTL translator (26LS32).

2. There should be a ground plane providing at least 75% coverage of the board. Particular care should be take with the filter, amplifier, and VCO components enclosed by the heavy black line.

3. +5 volt power supply should have low impedance to ground plane at each chip. This can be acomplished by a separate +5 volt ground plane (or grid) or bypassing of the +5 supply at each chip. Power supply bypass capacitors should have short leads and have a low inductance (less than 30 nH) path between +5 volts and the ground plane.

4. Discrete components should be located next to the IC chip with which they are associated.

5. VCO timing and bypass capacitors should be located as close to the chip (MC1658) as possible.

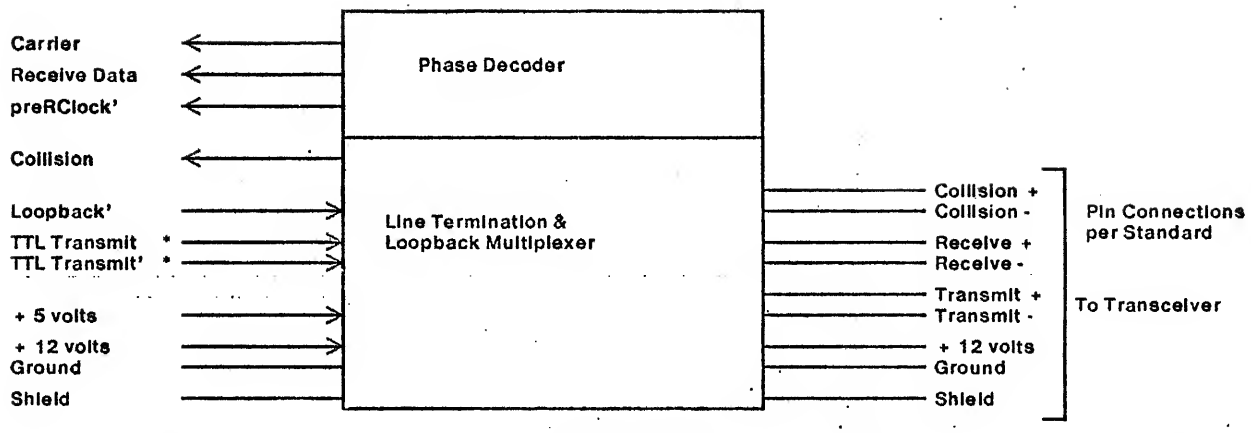
6. Use of SIP's (single inline package) for terminators may ease layout problems due to many nets converging on a single terminator package. (Might use 4 SIPs instead of 2 DIPs)

7. It is OK to rearrange gates, flip-flops, & amplifiers within a given IC package, but do not trade from one package to another. Circuit operation depends on matching of sections within a package.

8. Component variations in the MC1658 VCO make it necessary to adjust the capacitance of the timing capacitor on each unit. Units examined so far require a range from 77 pF to 95 pF. C1 + C2 (NPO temperature coefficient) and the adjustable capacitor must span a range of approximately 35 pF . The sum of C1 and C2 in parallel is used to center the trimmer in the middle of the necessary adjustment range. This is done at design time when the PC board is available. Two capacitor positions are available to permit using two capacitors to get the desired value.

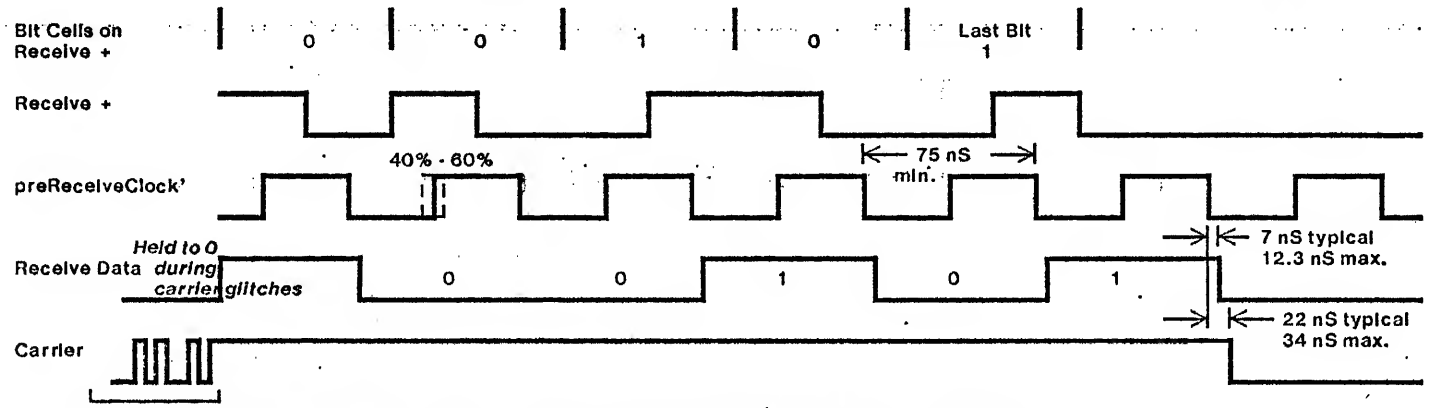
Adjustment

Adjustment is performed by connecting a 10 MHz input to the decoder and measuring the DC voltage between points T1 and T2. The board should be at room temperature and have power applied for at least 20 to 30 seconds before making the adjustment. The power supply voltage should be 5.0 volts + or - 100 mV and + 12 V + or - .25V. The adjustable capacitor is adjusted to set the voltage between points T1 and T2 to 10 mV or less. Measurement should be done with a DC voltmeter with 20,000 ohms/volt or greater input impedance. The data line should be checked to verify that it is in a stable 0 or 1 state and the carrier signal verified to be in a constant 1 state once the adjustment is made.



* TTLTransmit and TTLTransmit' are the true and complement outputs of the final 74S74 flip-flop in the phase encoder.

Block Diagram



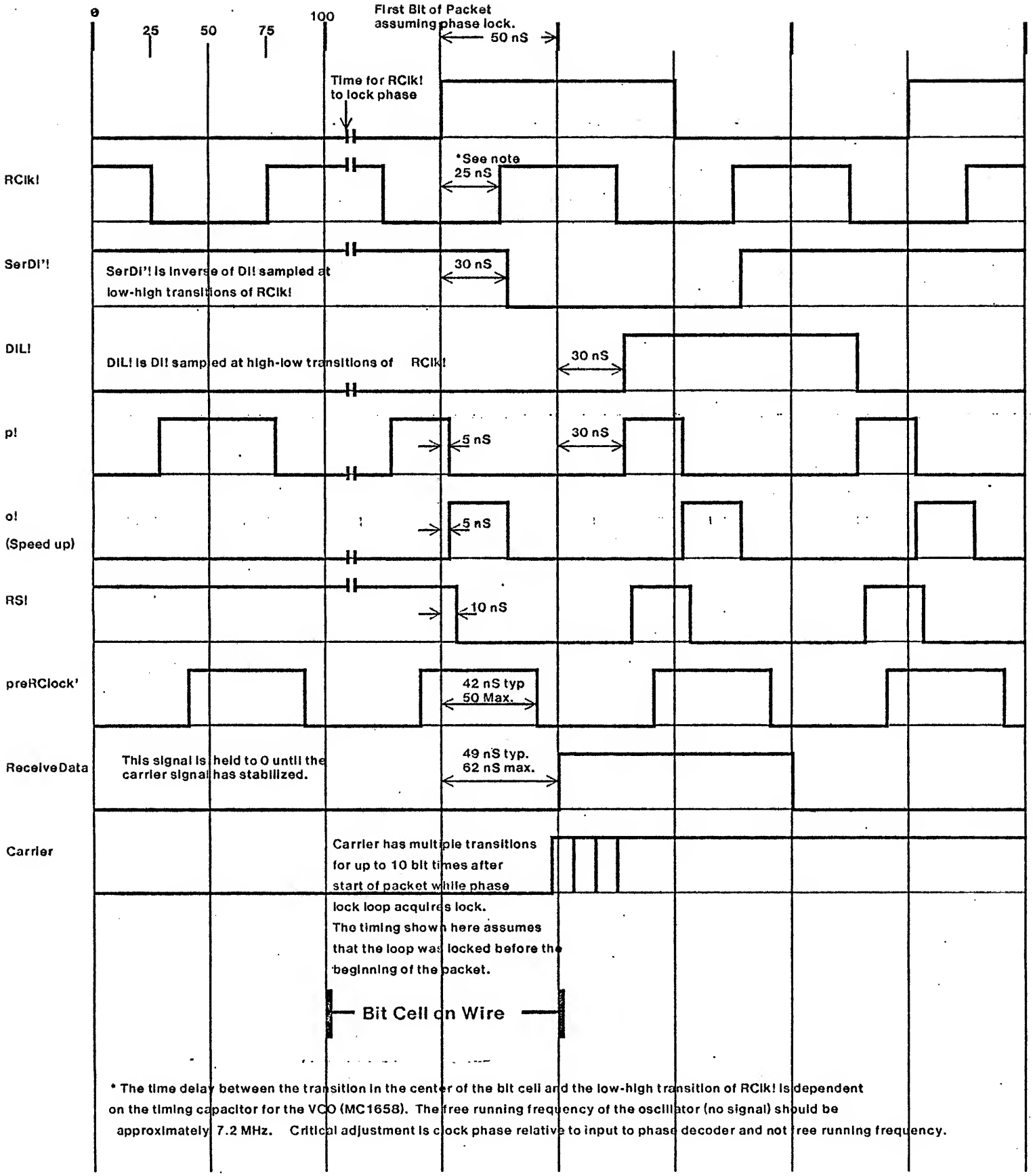
Carrier line has glitches at the start of carrier. The receive data line is held to zero during this period until the phase locked loop has acquired lock and the receive data stream contains valid data.

Interface Timing

1. preRClock' has a 40% to 60% duty cycle. It free runs at about 7.2 MHz. With the test generator and 5000 feet of cable, a bit cell can be shortened by as much as 20 nS. This results in a clock period jitter ranging from 83 nS to 122 nS. Logic design must work with a 75 nS minimum clock period.
2. The collision signal is a TTL version of the differential signal which has passed through the line compensation and envelope threshold circuits.
3. The TTLTransmit signals are routed to the transceiver interface unless loopback is asserted in which case it goes to the phase decoder.
4. When Loopback' = 1, the multiplexer sends TTLTransmit to the transceiver and it sends the receive signal from the transceiver to tha phase decoder. When Loopback' = 0, a logic 0 is sent to the transceiver and the TTLTransmit signal is sent to the phase decoder.
5. The 26LS32 can sink up to 8 mA in the logic low state. The 74S04 can sink up to 20 mA in the logic low state.
6. The differential signal, Transmit, has a differential voltage of .8 volt peak and a common mode voltage of 3.7 V above ground.
7. The differential receiver circuits for collision and receive require signals of at least .4 volt peak differential amplitude and a common mode voltage between 0 and +5 volts. None of the inputs to the line receiver circuits should fall outside the range of -.5 V to + 5.5 V.
8. The line receivers can withstand up to .1 volt noise on the differential signal leads. This is accomplished by the introduction of an offset voltage at the input of the line receiver when the circuit is in the quiescent state. This offset is removed if a signal larger than 300 mV is present at the input to the receiver. The offset will not return until 200 to 300 nS after the last high-low transition on the given signal pair. The offset will also return if there are no signals larger than .12 volt peak present on the line.
9. The phase locked loop in the phase decoder takes up to 16 bit times to acquire lock (typically 5).
10. Power - .7 A @ +5 volts, 2mA for interface and .5A for transceiver at +12 volts Both supply tolerances are + or - 5%.

Interface Specifications

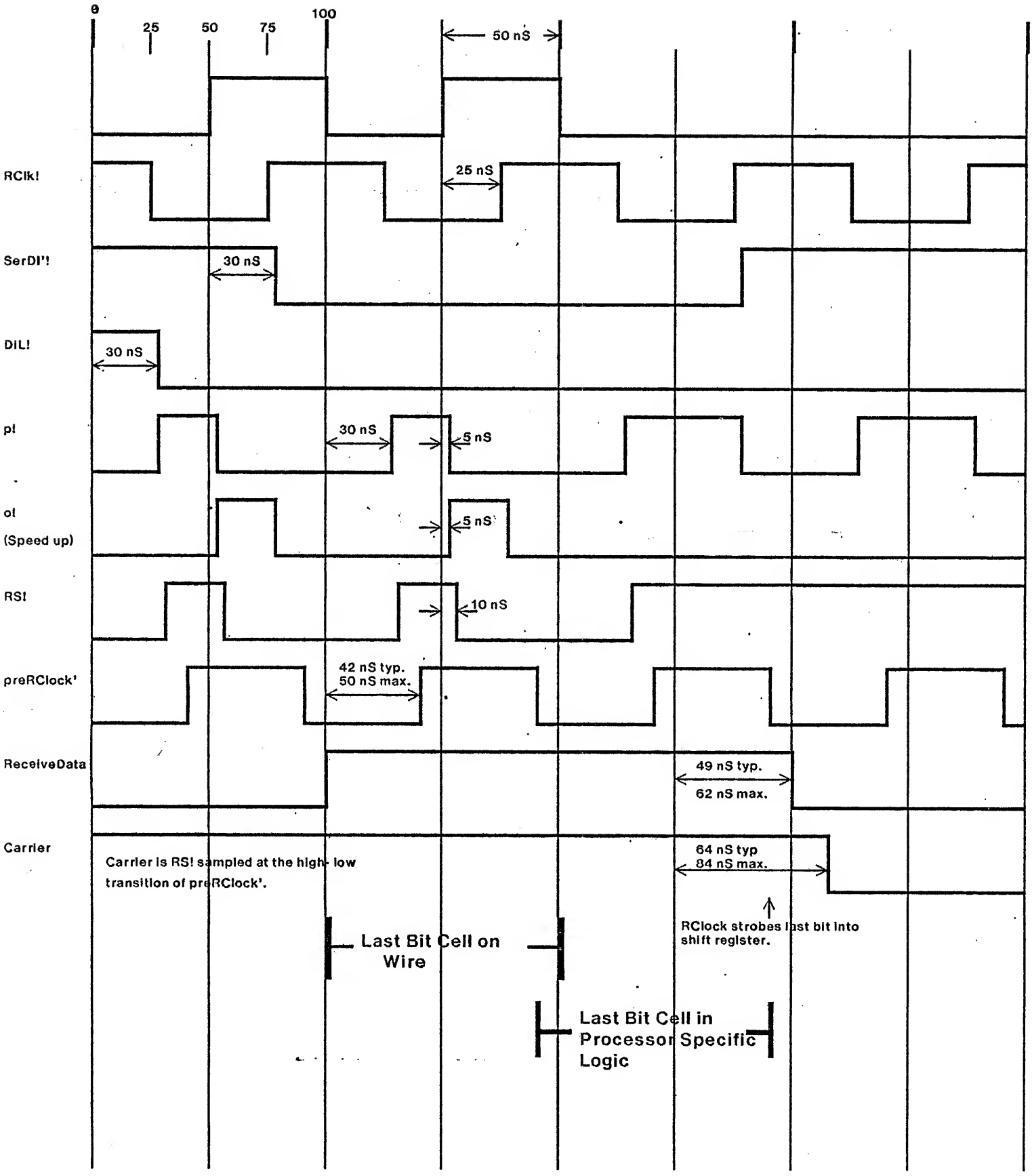
XEROX SDD	Project EN	Analog Electronics Block Diagram & Specs.	File Option52.sily	Designer Crane	Rev C	Date 6/23/80	Page 52



* The time delay between the transition in the center of the bit cell and the low-high transition of RClk! is dependent on the timing capacitor for the VCO (MC1658). The free running frequency of the oscillator (no signal) should be approximately 7.2 MHz. Critical adjustment is clock phase relative to input to phase decoder and not free running frequency.

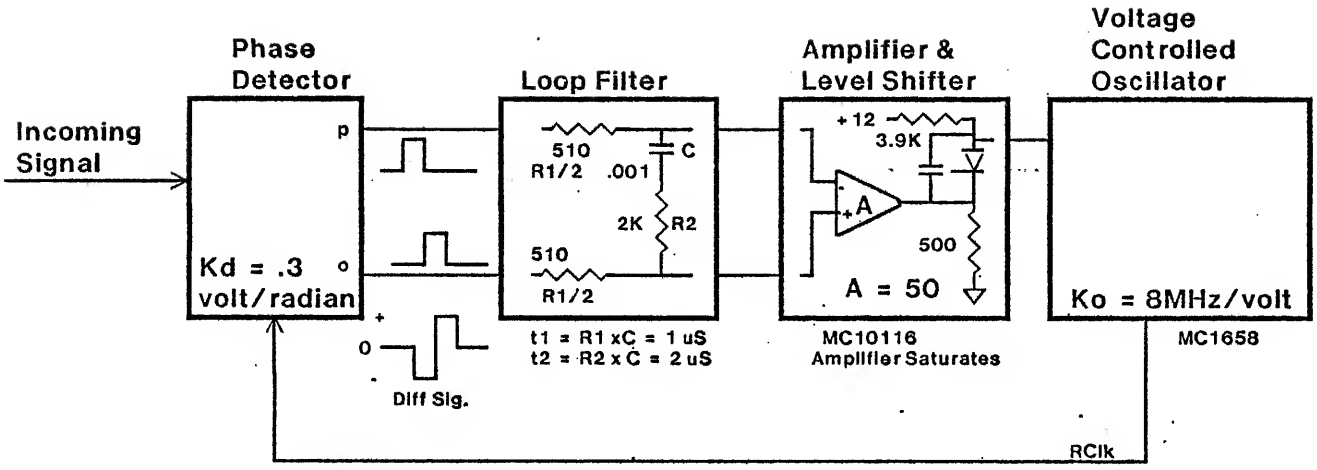
Time delays are from data book typicals & maximums. The number of significant digits is not an indication of accuracy.

XEROX SDD	Project EN	Receive Timing Start of Packet	File Option53.sily	Designer Crane	Rev C	Date 6/24/80	Page 53



Time delays are sums of typicals and maximums from data books. The number of significant digits is not an indication of accuracy.

XEROX SDD	Project EN	Receive Timing End of Packet	File Option54.sily	Designer Crane	Rev A	Date 6/24/80	Page 54



Natural Frequency $Wn = \sqrt{\frac{Ko\ Kd\ A}{t1 + t2}}$ = 7.9 MHz if Amplifier were linear for pulses A = 1 since amplifier saturates. Thus Wn = about 1 MHz.

Damping Factor $D = \frac{Wn}{2}\left[t2 + \frac{1}{Ko\ Kd\ A}\right]$ = about 6.28, but amplifier is not saturated when pulses are gone so this is not exactly correct either.

$Ko = 1.25 \times 10^{9}$ rad/volt

$Kd = .3$ volt/radian

$A = 50$ volts/volt

$t1 = 10^{-6}$ seconds

$t2 = 2 \times 10^{-6}$ seconds

Circuit Operation

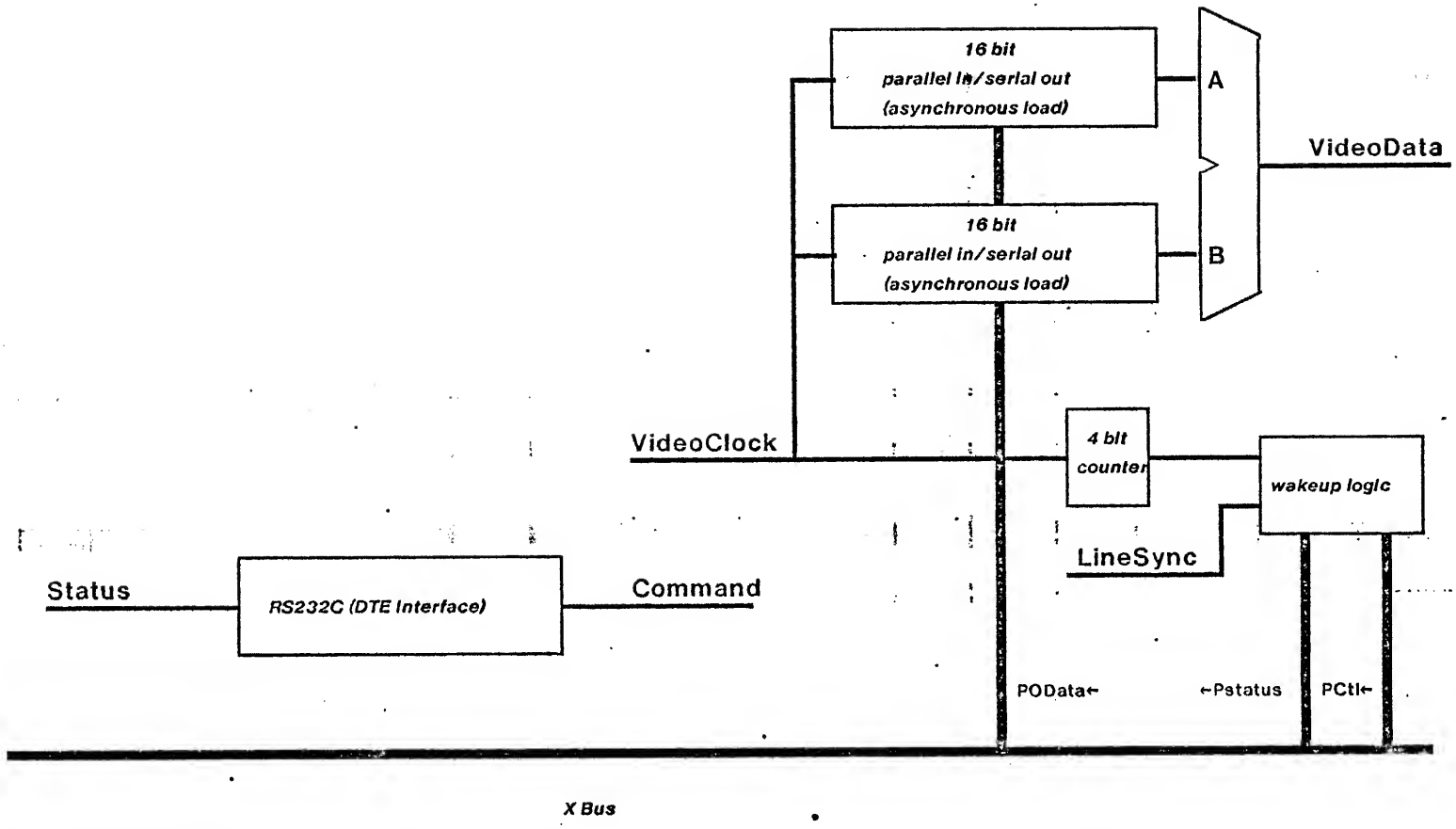
The figure above identifies the key parts of the phase locked loop. The details of the phase detector are not important here except for the outputs p and o. With no signal input, p has a 50% duty cycle and o is always low. When a signal appears, but is not yet locked, both p and o have duty cycles averaging 25% over many cycles. This produces a zero net input to the amplifier and VCO. The VCO is tuned such that this voltage causes the VCO to run near 10 MHz. Assuming that the input signal is at 10MHz, the PLL will be well within its lock range. In the locked state, if the input signal advances in phase, the o signal will become wider and the p signal will get shorter causing a net positive voltage over the cycle. This causes the VCO to increase in frequency and catch up. The loop filter provides some attenuation of quick phase shifts, but most importantly it, combined with the high amplifier gain, centers the local clock (VCO) at 90 degrees with respect to the incoming signal. Note that in the locked state, both p and o have a 25% duty cycle in every cycle rather than 25% averaged over many cycles.

Parts Selection & Design Comments

The key linear components of the phase locked loop, the amplifier and VCO, were selected to be readily available and operate from a + 5 volt supply. The Motorola MC10116 amplifier and MC1658 VCO were selected. The combination of these two components with the diode level shifter provides a constant output frequency for a given differential input in the face of varying power supply voltage and temperature. It is important that the amplifier (MC10116) not have power supply compensation like the Fairchild 10K logic series. Motorola or Signetics parts should be used. The Fairchild part should NOT be used.

Limited linear range of amplifier (.8 volts peak-peak) requires that textbook equations have correction factors added. Some analysis and experimentation have resulted in the above circuit configuration. In particular, the typical integrator configuration works poorly because the amplifier saturates and fails to charge the integrator capacitor.

Because the pulses from the phase detector pass directly to the VCO, typical lock time of this circuit is very short. These pulses at the VCO are also the reason for the 40% to 60% duty cycle of the clock waveform.



Signals from LSEP connector are in the large font.

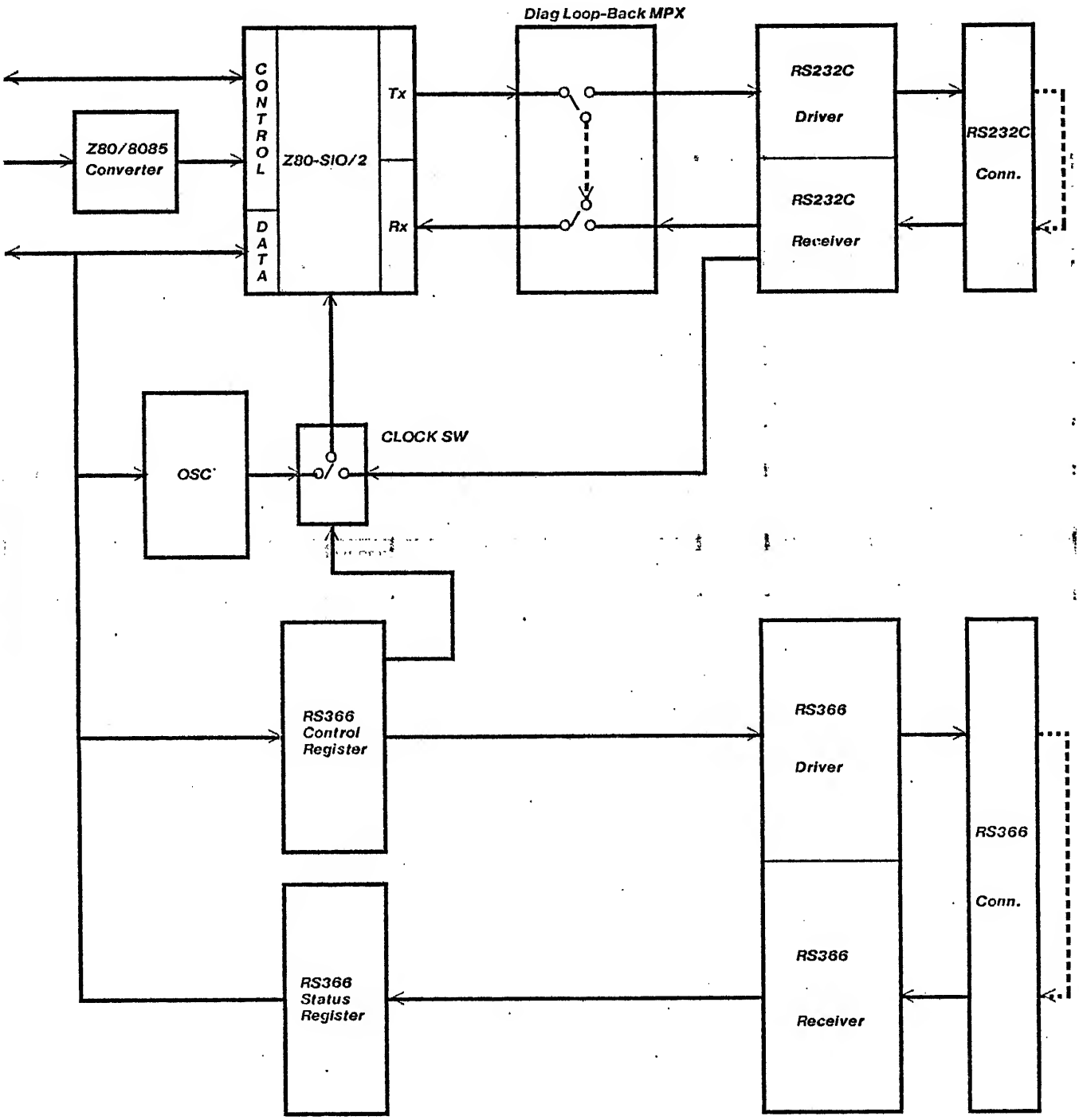
Control Register Functions:

1. disable wakeup (level)
2. clear buffer (level)
3. test mode (level)
4. end of line (pulse)
5. clear errors (pulse)
6. step (test mode clock)

Status Register:

1. data overrun
2. buffer loadable (0 = >A, 1 = >B)
3. VideoData

XEROX SDD	Project Dandelion	Reference LSEP Block Diagram	File Option80.sily	Designer Jarvis	Rev C	Date 3/11/80	Page 80



XEROX SDD	Project Dandelion	Title RS-232-C Interface Block Diagram	File Option90.sily	Designer K.Yamanaka	Rev C	Date 6/9/80	Page 90

RS232C Loop Back Plug (Plug1)

From	OutPut Signal Name	To	Input Signal name
P2-2	Transmitted Data *(DCE source)*	P2-3	Received Data *(DCE Input)*
P2-4	Request to Send	P2-5	Clear to Send
P2-4	Request to Send	P2-8	Receive Line Signal detector
P2-19	Secondary Request to Send	P2-12	Secondary Received Line Signal Detector
P2-14	Secondary Transmitted Data *(DCE source)*	P2-16	Secondary Received Data *(DCE Input)*
P2-19	Secondary Request to Send	P2-13	Secondary Clear to Send
P2-20	Data Terminal Ready	P2-6	Data Set Ready

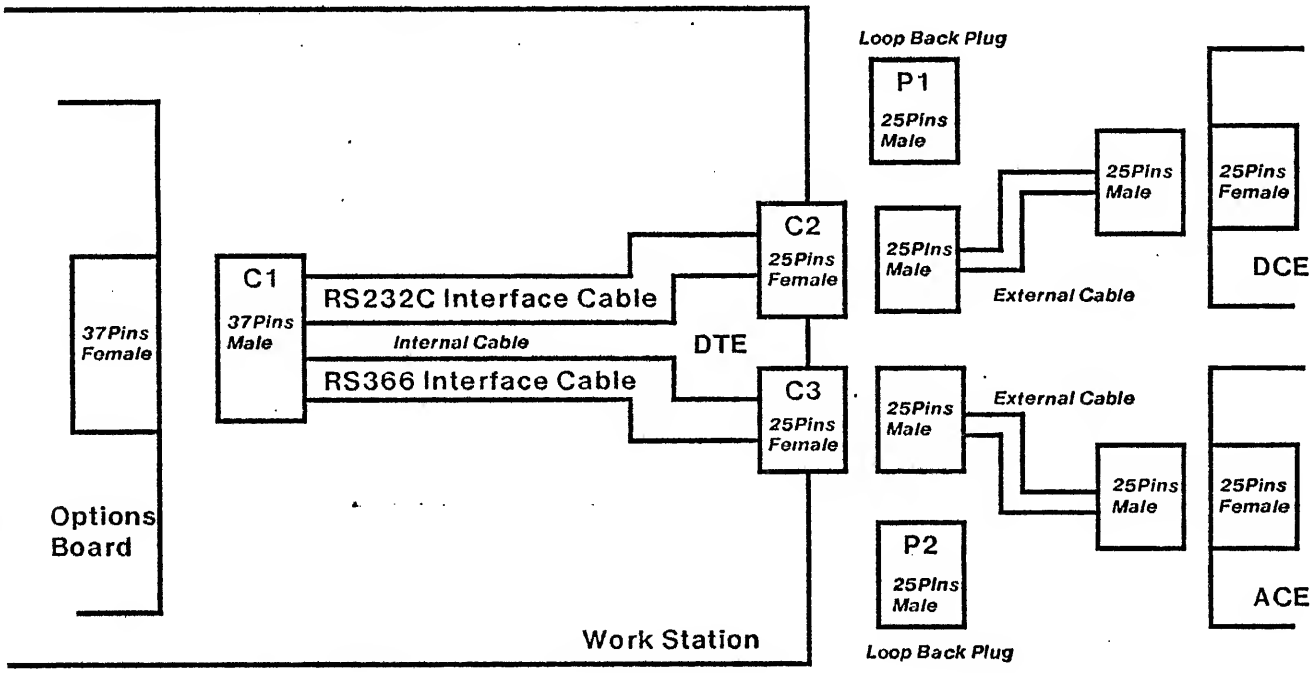
Unused Signals:

P2-15	Transmittion Signal Element Timing	*(DCE source)*
P2-17	Receiver Signal Element Timing	*(DCE source)*
P2-22	Ring Indicator	
P2-24	Transmit Signal Element Timing	*(DTE source)*

RS366 Loop Back/ LSEP Plug (Plug2)

From	OutPut Signal Name	To	Input Signal name
P3-14	Number Bit1 (RS366)	P3-6	Power Indication (RS366)
	Command! (LSEP)	P3-10	Status! (LSEP)
P3-15	Number Bit2 (RS366)	P3-3	Abondon Call & Retry (RS366)
	Command'! (LSEP)	P3-11	Status'! (LSEP)
P3-16	Number Bit4	P3-13	Call origination Status
P3-17	Number Bit8	P3-5	Present Next Digit
P3-2	Digit Present	P3-22	Data Line Occupied

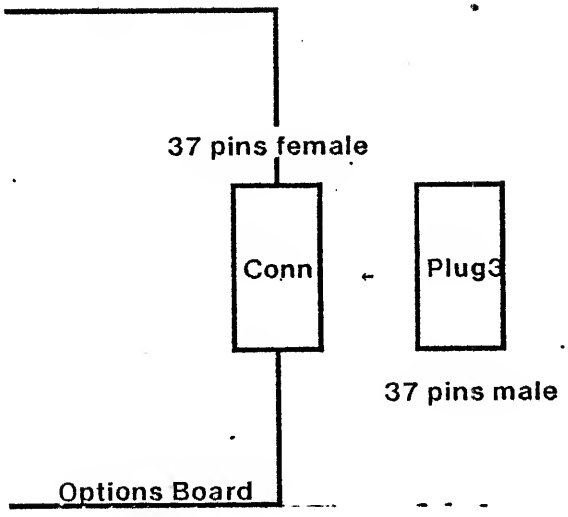
Unused Signal P3-4 Call Request



XEROX SDD	Project Dandelion	Title Loop-Back Connector Int/Ext Cable Connector	File Option91.sily	Designer K.Yamanaka	Rev C	Date 7/11/80	Page 91

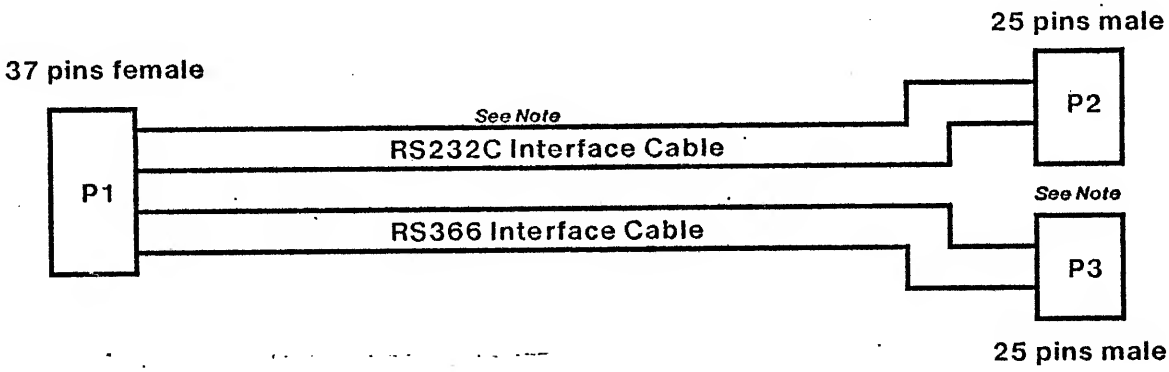
Loop Back Plug (Plug3)

From	Signal Name (OUTPUT)	to	Signal Name (INPUT)
2 (152)	PrimTData'	3 (153)	PrimRData'
4 (154)	PrimRTS	5 (155)	PrimCTS
4 (154)	PrimRTS	8 (158)	PrimLineDet
25 (175)	SecndRTS	12 (162)	SecndLineDet
20 (170)	SecndTData'	22 (172)	SecndRData'
25 (175)	SecndRTS	13 (163)	SecndCTS
26 (176)	DTReady	6 (156)	DataSetRdy
15 (165)	NB1'	18 (168)	PWI
34 (184)	NB2'	29 (179)	ACR
33 (183)	NB4'	16 (166)	COS
32 (182)	NB8'	19 (169)	PND
28 (178)	CRQ	9 (159)	RingInd (RS232C Signal)
30 (180)	DPR	37 (187)	DLO



XEROX SDD	Project	Title	File	Designer	Rev	Date	Page
	Dandelion	Loop-Back Plug (2)	Option92.sily	K.Yamanaka	C	7/8/80	92

From	Signal Name at P1	To	RS232C/RS366 Interface Signal Name
24		P1-27	
36		P1-35	
1 (151)	GND	P2-1	Protective Ground
2 (152)	PrimTData'	P2-2	Transmitted Data *(DCE source)*
3 (153)	PrimRData'	P2-3	Received Data *(DCE input)*
4 (154)	PrimRTS	P2-4	Request to Send
5 (155)	PrimCTS	P2-5	Clear to Send
6 (156)	DataSetRdy	P2-6	Data Set Ready
7 (157)	GND	P2-7	Signal Ground
8 (158)	PrimLineDet	P2-8	Receive Line Signal detector
9 (159)	RingInd	P2-22	Ring Indicator
10 (160)		P2-11	
11 (161)	*Spare* (Option)	P2-24	Transmit Signal Element Timing *(DTE source)*
12 (162)	SecndLineDet	P2-12	Secondary Received Line Signal Detector
13 (163)	SecondCTS	P2-13	Secondary Clear to Send
20 (170)	SecndTData'	P2-14	Secondary Transmitted Data *(DCE source)*
21 (171)	DCETxClk	P2-15	Transmittion Signal Element Timing *(DCE source)*
22 (172)	SecndRData'	P2-16	Secondary Received Data *(DCE input)*
23 (173)	DCERxClk	P2-17	Receiver Signal Element Timing *(DCE source)*
25 (175)	SecndRTS	P2-19	Secondary Request To Send
26 (176)	DTReady	P2-20	Data Terminal Ready
31 (181)	*Spare*		
28 (178)	CRQ	P3-4	Call Request
29 (179)	ACR	P3-3	Abondon Call & Retry
30 (180)	DPR	P3-2	Digit Present
14 (164)	GND	P3-1	Frame Ground
15 (165)	NB1'	P3-14	Number Bit1
16 (166)	COS	P3-13	Call origination Status
17 (167)	GND	P3-7	Signal Ground
18 (168)	PWI	P3-6	Power Indication
19 (169)	PND	P3-5	Present Next Digit
32 (182)	NB8'	P3-17	Number Bit8
33 (183)	NB4'	P3-16	Number Bit4
34 (184)	NB2'	P3-15	Number Bit2
37 (187)	DLO	P3-22	Data Line Occupied



Note: For P2 and P3, Cannon or Cinch type DB-19604-432(male) associated with Cinch type DB-521226-1 HOOD.

Note: Use 24 AWG Stranded, Non twisted paire wire for fabrication.

XEROX SDD	Project: Dandelion	Title: Cable Connection	File: Option93.sily	Designer: K.Yamanaka	Rev: C	Date: 5/23/80	Page: 93

Rev A (5/28/80)

Created

Rev B (6/27/80)

Add Power supply section of Z80-SIO/2 (m8p).

Add inverter d14d.

Signal name change from PrCTS' to SecCTS'.

Signal name change from SecCTS' to PrCTS'.

Move signal "DataTermRdy'" of Z80-SIO/2 from pin16 to pin 25.

Change IC SN74LS257 to SN74LS157

Change IC from SN7437N to SN7438N

SIOHigh1 is pull-up ed by 1k ohm.

1 10 20 30 40 50 51 60 70 80 90 100
101 110 150 151 200

LSEP

	a	b	c	d
	S02 @ pWait,pAlwys ElData,...	S374 @ AlwaysClk	S241 BufX[0-7]	S241 BufX[8-15]
18	LS74 Load,Want	S51 Req,ShiOut	LS165 BufA[0-7]	LS165 BufA[8-15]
17	LS74 Swap,Data	LS74 Line, Ref	LS165 BufB[0-7]	LS165 BufB[8-15]
16	LS163 VWord		LS04 POD,PCtl,EWr ElCtl,EOCt,EOD	LS175 PCtl
15	LS32 @ ...,TRd, TWr,...		LS02 @ Clr,Need, ...,...	LS32 Wr', Rd', ClkLp, ClrBuf'
14		LS273 RS366 Ctl	LS04 dmaA,B,Int, iorQ,CE,CD	LS245 BaudByte
13		LS245 SIOData	LS240 RS366 Stat	LS245 LSEPByte
12	a: I8253 LSEP Baud Rate Gen		b: m12	c: i8251 LSEP UART
11			LS10 @ SIOCE,CD', ...	
10			S37 @ SIOClk' SIOHIgh	LS00 IOPReset' BA', IORQ, SIOBA
9	LS157 LoopBack	LS157 LoopBack	LS157 LoopBack	LS157 LoopBack
8	a		b: m8	c: Z80-SIO/2 RS232 Serial
7				LS74 Ring, Coil
6				
5				
4	PLAT16 LSEPTerm2		N75188 RS232 Drv	
3	PLAT16 LSEPTerm1		N75188 RS232 Drv	N75188 RS366 Drv
2	MC124 LSEP: Comm, Data		N75189 RS366 Rcv	N75189 RS232 Rcv
1	MC125 LSEP: Clk, Sync, Stat		N75189 RS366 Rcv	N75189 RS232 Rcv
	a	b	c	d

ETHERNET

	e	f	g	h	i
19	S240 EStat[0-7]	S374 ElData[0-7]	S299 TData[0-7]	S225 Buf[0-3]	
18	S240 EStat[8-15]	S374 ElData[8-15]	S299 TData[8-15]	S225 Buf[4-7]	S374 @ AlwaysClk
17	LS175 ElCtl	LS374 EOData[0-7]	LS374 RHold[0-7]	S225 Buf[8-11]	LS175 StatusHold
16	LS175 EOCtl	LS374 EOData[8-15]	LS374 RHold[8-15]	S225 Buf[12-15]	LS175 RStatus
15	S00 ElData,EOData, ElCtl~,EOCtl~	S51 WrBuf', Attn'	S299 RData	S64 RdBuf'	S64' EReq'
14	S10 LSEP Qual	S10 LdRHold.H, L LdRStatus	S04 @ RCO,atn,EID, ...,...,alwys	LS175 RcvState	LS175 @ RClock
13	LS74 TickElapsed, OverRun	LS163 RcvCnt	S00 @ PPkt,RC = 15', BDs.3	F93453 RcvProm	LS374 RSync
12	e: F93453 TrnProm	f: S10 PreamDet', RcvCnt = 7', TrnCnt = 7'	g: LS163 TrnCnt	h: S51 PktInMode' TRClk'	
11	S175 TrnState	S374 Tsync	F93453 TrnEndProm	LS163 WaitB	LS163 WaitA
10	S10 TrnMode, TrnInit, c4'	S374 Tclock		LS393 DeferCnt	LS00 DC = 384, ClrDC,bw', RdyTrn
9	S08 @ Snd,SetCRC, PhG,....	S00 @ POM,TrnCRC, c7,...	S02 StTrn,Under, rsc,SetCRC	LS04 @ Full,Car,EW TC = 15,	S253 TrnMux
8	e: S30 c5'	f: S260 c1,GoodCRC	g: S30 c6'	h: S260 c2,c3	
7	LS244 Testability	S86 PhE,0x,1x,3x	S86 4x,6x,7x,9x,	S86 10x, 11x, 15x, 21x	S86 22x, 25x, 32a, 32b
6	K1114A 20 MHz	LS273 CRC[0-7]	LS273 CRC[8-15]	LS273 CRC[16-23]	LS273 CRC[24-31]
5	S74 Trn, pTClock	LevelPlat		S04 TClk,TBit, c32,RBit, RclkSh,RClk	
4	MC231 RS, Car	MC231 SerDI, DiL	MC102 DI, Transmit	26LS32 Coll, RBit', Car, pRClk	
3	FilterPlat	MC103 dr, rbe',Lp	MC102 p, o	MiscPlat	CollPlat
2	MC116 ppp,Amp, Ref	VCOPlat	500 ohm ENTerm1	500 ohm ENTerm2	RcvPlat
1	MC1658 VCO	TrimPlat	MC115 RComp,RcvE, CComp,ZComp	MC116 TrnE,Rcv+ Trn+	EPLAT
	e	f	g	h	i

No TTL In Box!!

DIP Orient.

I/O Connector Area (Top)

I/O Connector Area (Bottom)

XEROX SDD	Project Dandelion	Options Card Layout (Stichweld)	File Option99.sily	Designer Garner, Jarvis/Yamanaka	Rev C	Date 20 July 80

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MATERIAL LIST

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Rev. C

Dwg. No.

Drawing Title

Preliminary

Dandelion Options Card Parts List

[Iris]<Workstation>Options>OPTParts-C.dm

Model No.

Date 31 July 80

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ML

Item No.	Drawing Title		Drawing No.	No. Req.	Remarks
	Integrated Circuit	SN74S00	*733W00318*	3	
		SN74S02	*733W01643*	3	
		SN74S04	*733W00319*	2	
		SN74S08	*733W01611*	1	
		SN74S10	*733W01606*	4	
		SN74S30	*733W01645*	2	
		SN74S37	*733W02136*	1	
		SN74S51	*733W01621*	3	
		SN74S64	*733W01620*	2	
		SN74S74	*733W01771*	1	
		SN74S86	*733W01648*	4	
		SN74S175	*733W01630*	1	
		SN74S225	*733W01533*	4	*TI FIFO*
		SN74S240	*733W01633*	2	
		SN74S241	*733W01634*	2	
		SN74S253	*733W01636*	1	
		SN74S260	*733W00321*	2	
		SN74S299	*733W01668*	3	
		SN74S374	*733W01640*	6	
		SN74LS00	*733W01671*	2	
		SN74LS04	*733W01672*	3	
		SN74LS10	*733W01761*	1	
		SN74LS32	*733W01705*	2	
		SN74LS74	*733W01675*	5	
		SN74LS157	*733W01745*	4	
		SN74LS163	*733W01770*	5	
		SN74LS175	*733W01642*	7	
	Integrated Circuit	SN74LS165	*733W01674*	4	

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Drawing Title

Dandelion Options Card Parts List

[Iris]<workstation>Options>OPTParts-C.dm

Model No.

Date 31 July 80

Sheet 2 Of 4

Item No.	Drawing Title		Drawing No.	No. Req.	Remarks
	Integrated Circuit	LS240	*733W01625*	1	
		LS244	*733W01626*	1	
		LS245	*733W01740*	3	
		LS273	*733W01624*	5	
		LS374	*733W01698*	5	
		LS393	*733W01663*	1	
		Am26LS32		1	
		F93453	*733W01544*	3	*1Kx4 60nS*
		i8251A	*733W01600*	1	
		i8253-5	*733W02225*	1	
		Z80-SIO/2		1	
		SN75188	*733W01911*	3	
		SN75189	*733W00098*	4	
		MC1658		1	*No power supply compensation Motorola, Plessey??*
		MC10102	*733W01680*	2	
		MC10103	*733W01782*	1	
		MC10115		1	
		MC10116		2	*Mortorola or Signetics only. (Not Fairchild--because of its power supply compensation)*
		MC10124	*733W01682*	1	
		MC10125	*733W01685*	1	
	Integrated Circuit	MC10231	*733W01734*	2	

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Drawing Title

Dandelion Options Card Parts List

[Iris]<Workstation>Options>OPTParts-C.dm

Model No.	Date	Sheet
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ML

Item No.	Drawing Title		Drawing No.	No. Req.	Remarks
	Resistor 1/4 watt 5%	36 ohm	*703W28788*	6	
		68 ohm		4	
		110 ohm	*703W29988*	1	
		220 ohm	*703W30688*	5	
		240 ohm	*703W30788*	5	
		300 ohm	*703W30988*	1	
		510 ohm	*703W31588*	3	
		680 ohm	*703W31888*	2	
		1K ohm	*703W32288*	10	
		1.3K ohm	*703W32588*	3	
		2.0K ohm	*703W32988*	1	
		3.9K ohm	*703W33688*	1	
		10K ohm	*703W34688*	1	
	Resistor 1/4 watt 5%	15K ohm	*703W35088*	2	
	Resistor 1/4 watt 1% metal film	301 ohm	*703W15206*	4	
		475 ohm	*703W17106*	4	
		931 ohm	*703W19906*	1	
		1130 ohm	*703W20706*	1	
	Resistor 1/4 watt 1% metal film	1300 ohm	*703W21306*	4	
	Resistor Network 5% 15 pulldowns	510 ohms		2	*AB 316A511 ??*
	Diode	1N4148	*707W00273*	1	
	Fuse	10A slow blow	*708W11402*	1	
	Inductor	4.7 uH .55 ohm DC res.	*705W00021*	1	*Nytronics SWD 4.7*
	20 MHz oscillator	K1114A		1	

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Dandelion Options Card Parts List

Ethernet Phase Decoder

[Iris]<Workstation>Options>OPTParts-C.dm

Model No.	Date	Sheet
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ML

Item No.	Drawing Title	Drawing No.	No. Req.	Remarks
	Capacitor 6V, tantalum electrolytic, 33 uF		1	*Across 5V*
	Al Foil Electrolytic, 50 uF	*702W14201*	2	
	50V, Ceramic, .1 uF -20 + 80%	*702W05218*	~50	
	Capacitor 25V,_+ 30ppm NPO, 62pF + 5%		1	
	Capacitor, Adjustable 8.5-50 pF , 650 ppm TC			*JFD # MT550*
	Capacitor, 25V,_+ 30 ppm NPO 4.7 pF_+ 10%		2	
	10 pF_+ 10%		1	
	68 pF_+ 10%	*702W01191*	5	
	270 pF_+ 10%	*702W01891*	2	
	.001 uF + 10%	*702W02591*	2	
	Capacitor, 25V,_+ 30 ppm NPO .002 uF + 10%		2	
	15 Pin Female D series connector		1	AMP 206914-1